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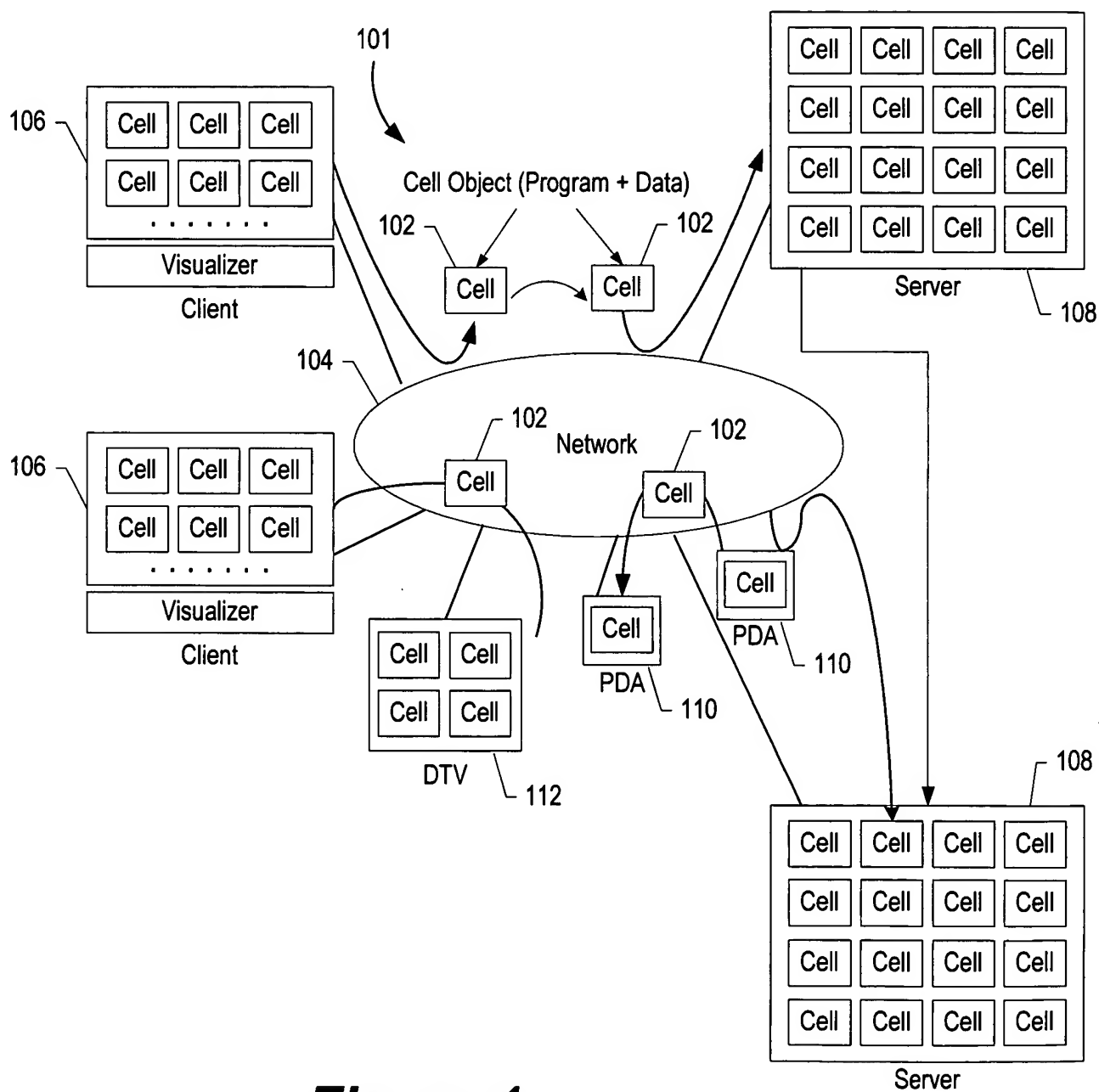
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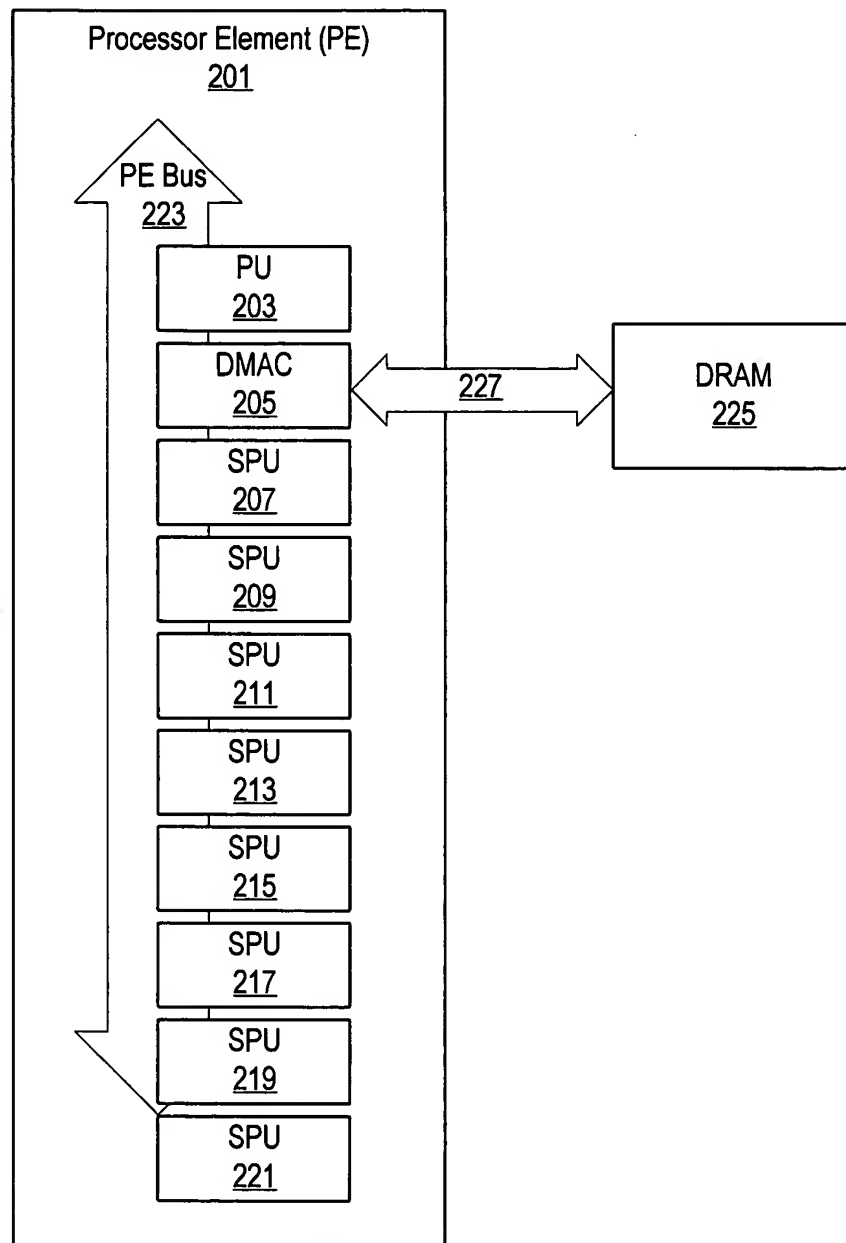
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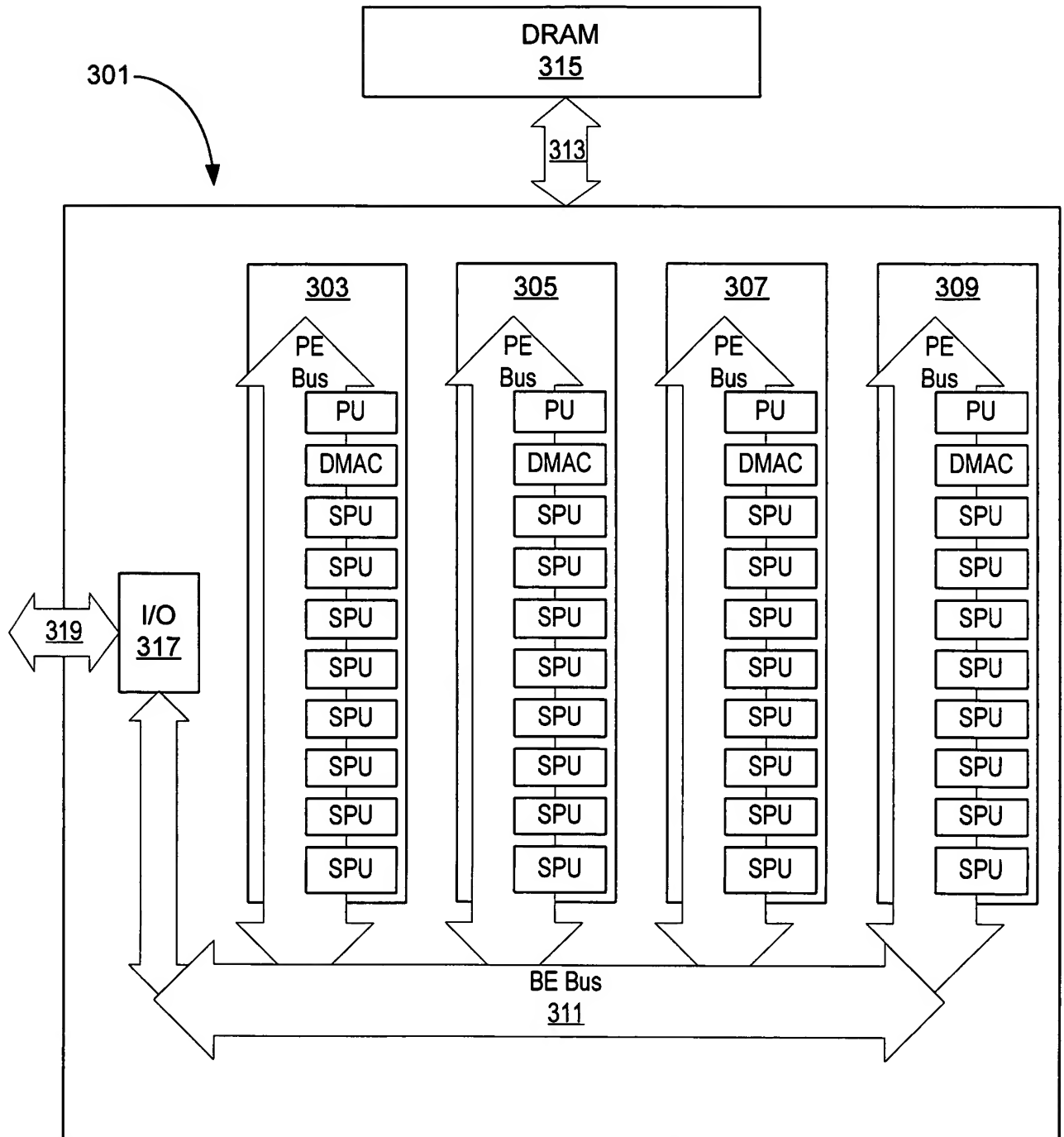
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**Figure 1**

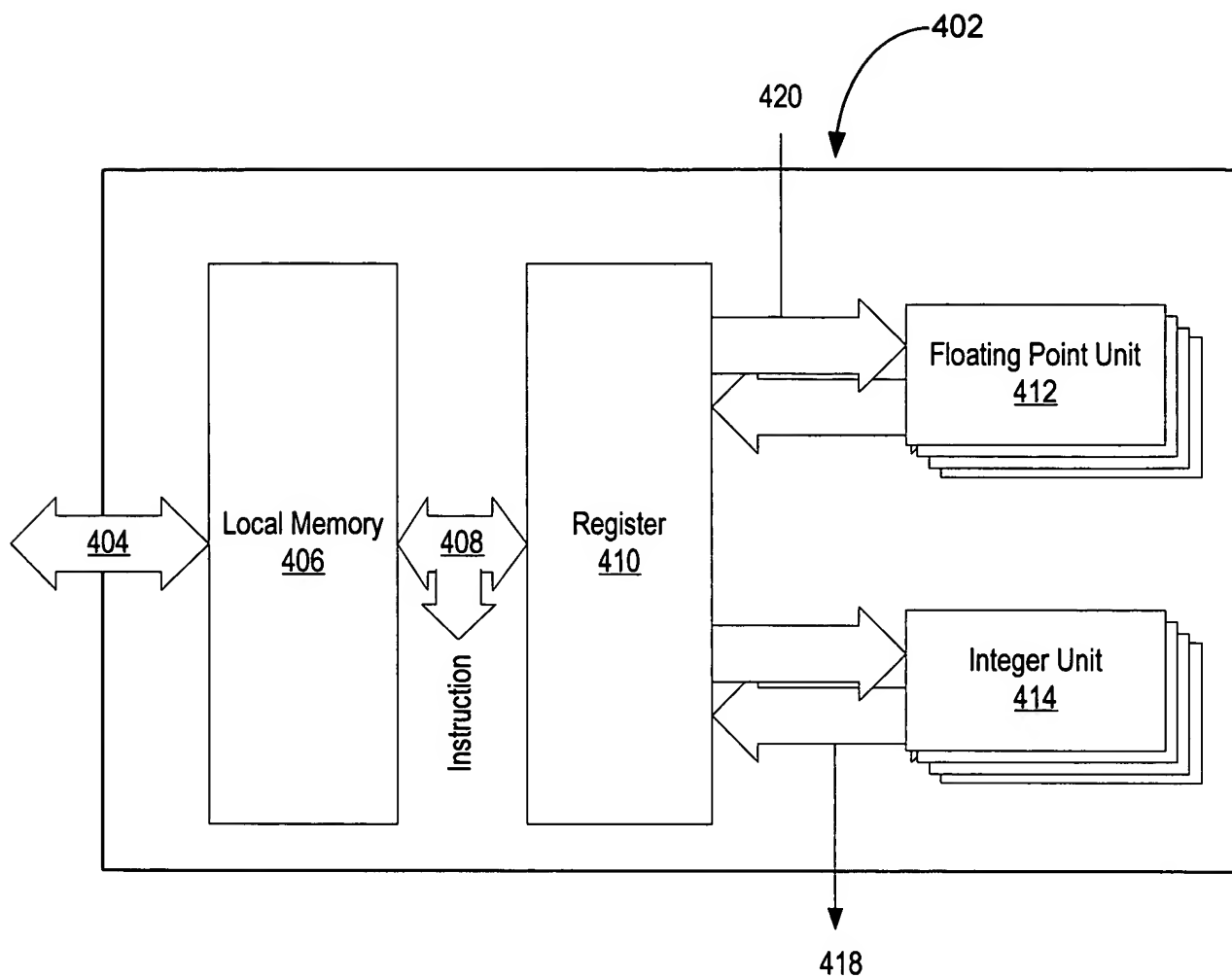
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**Figure 2**

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**Figure 3**

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**Figure 4**

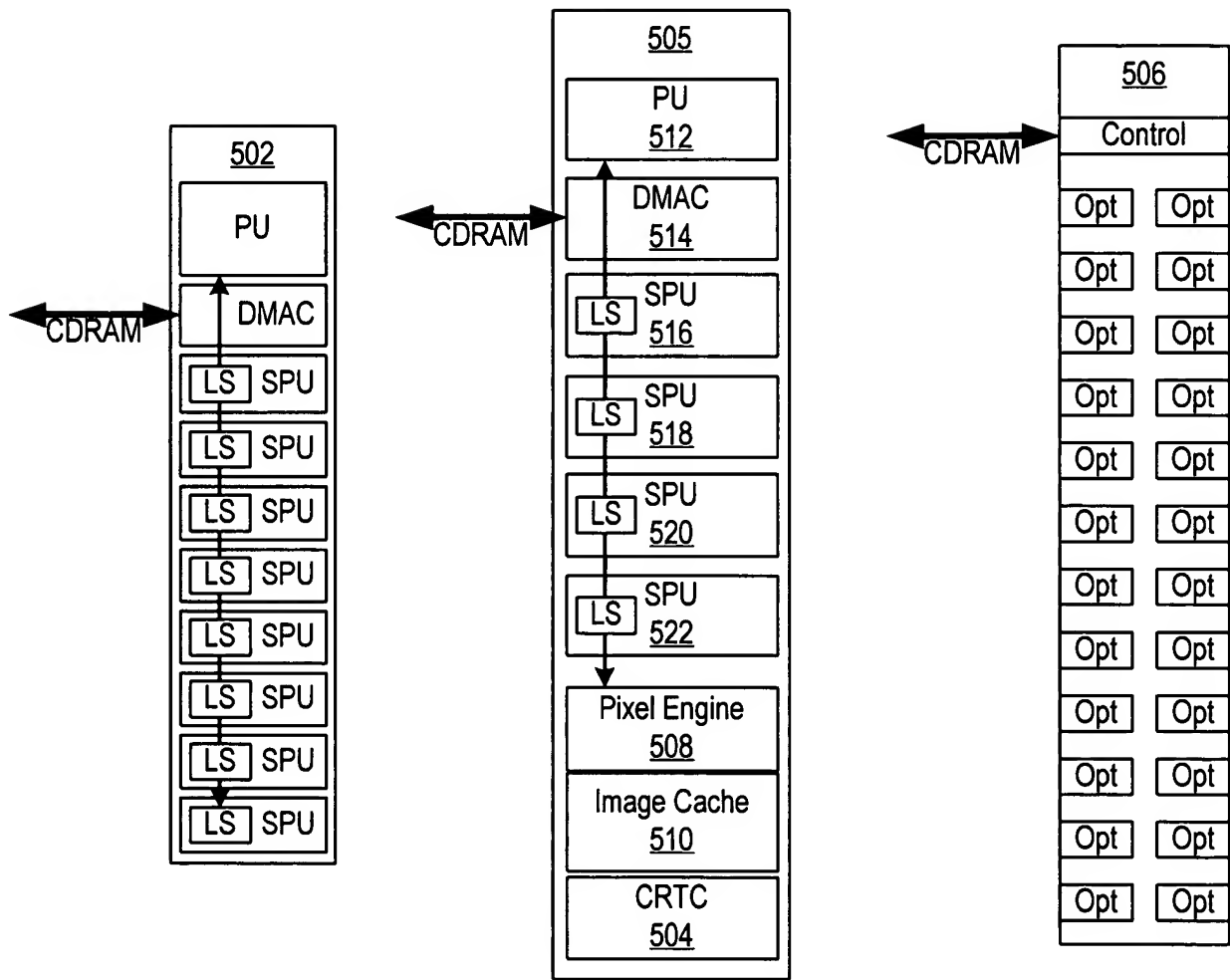
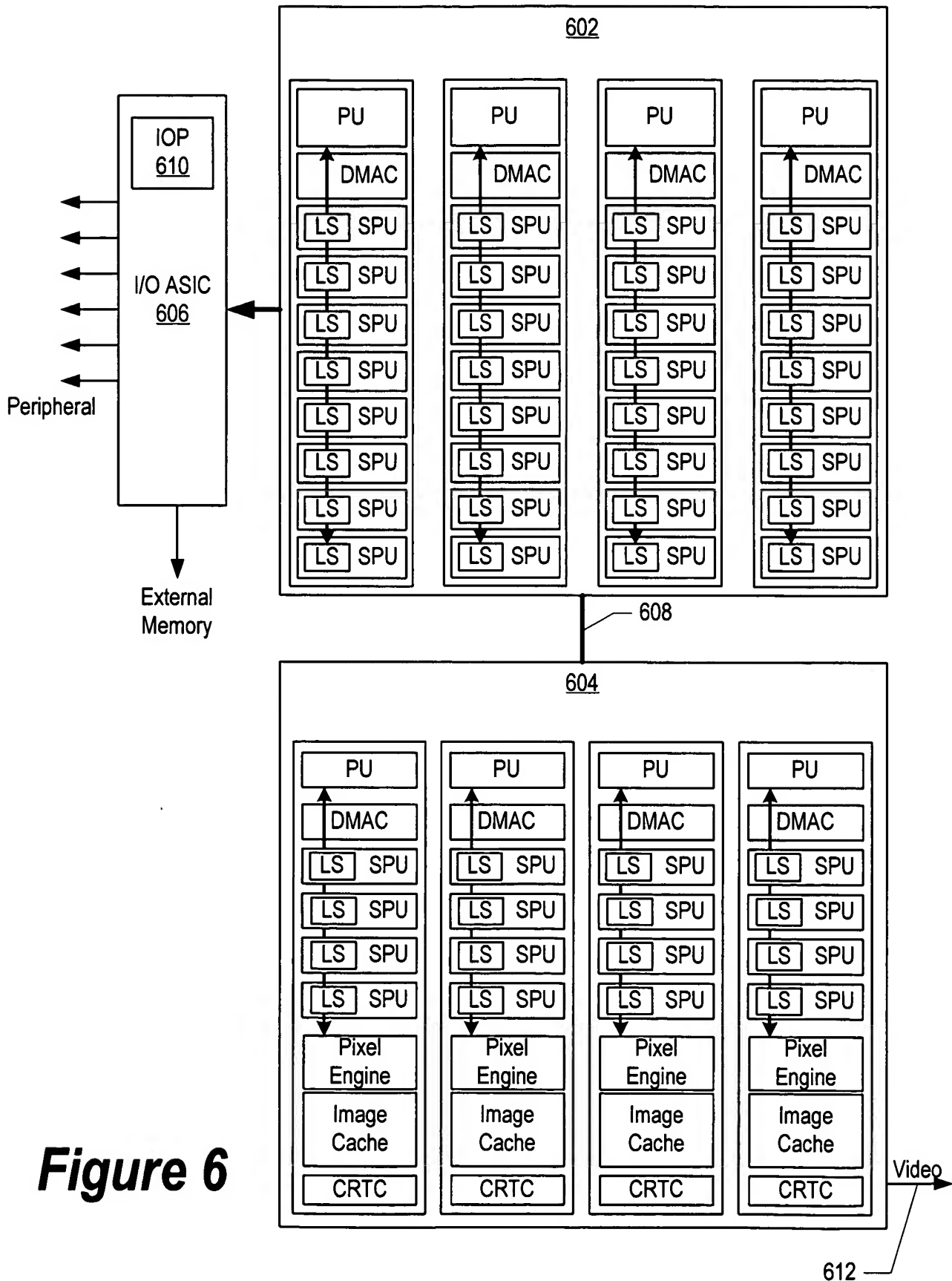
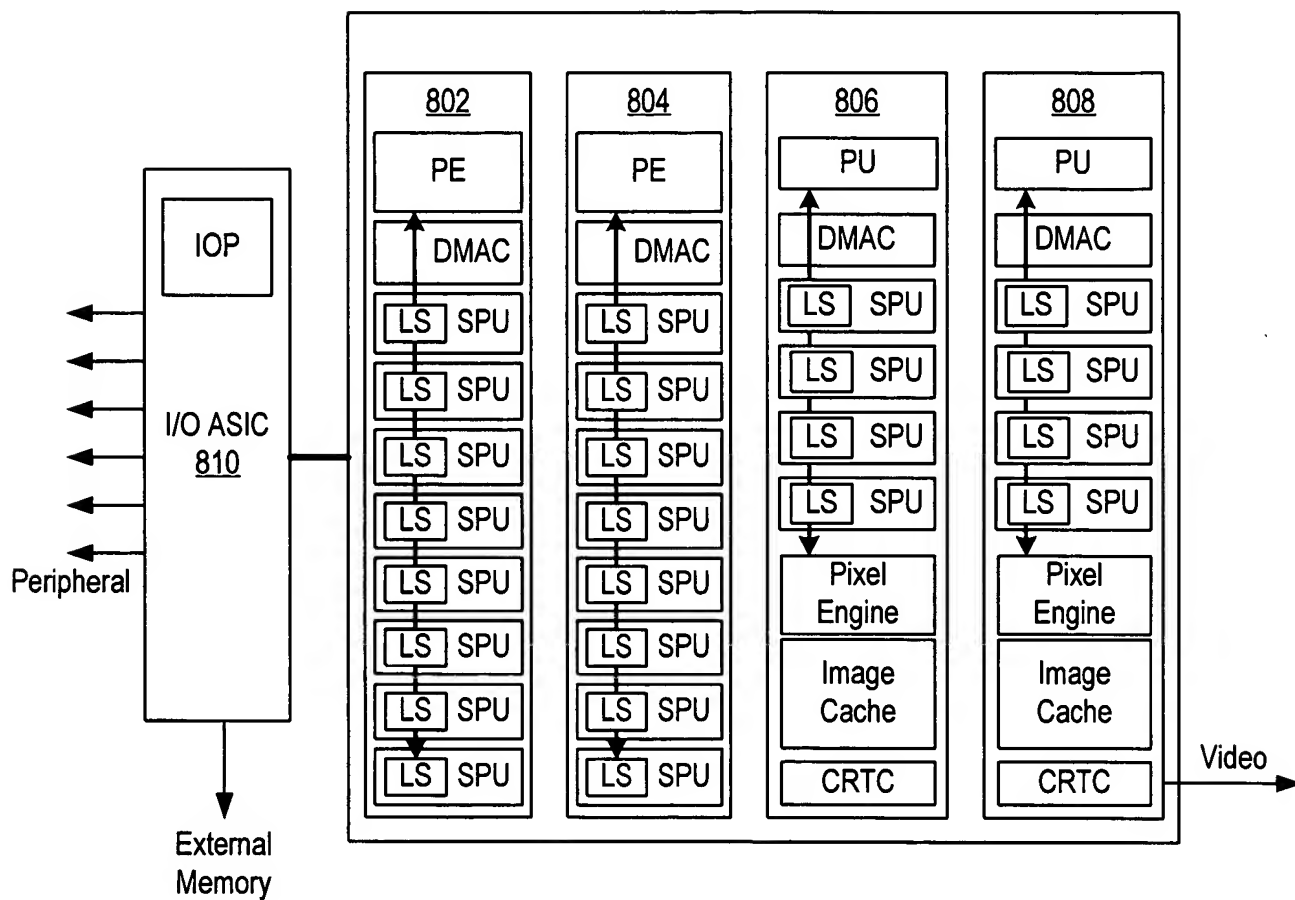


Figure 5





**Figure 8**

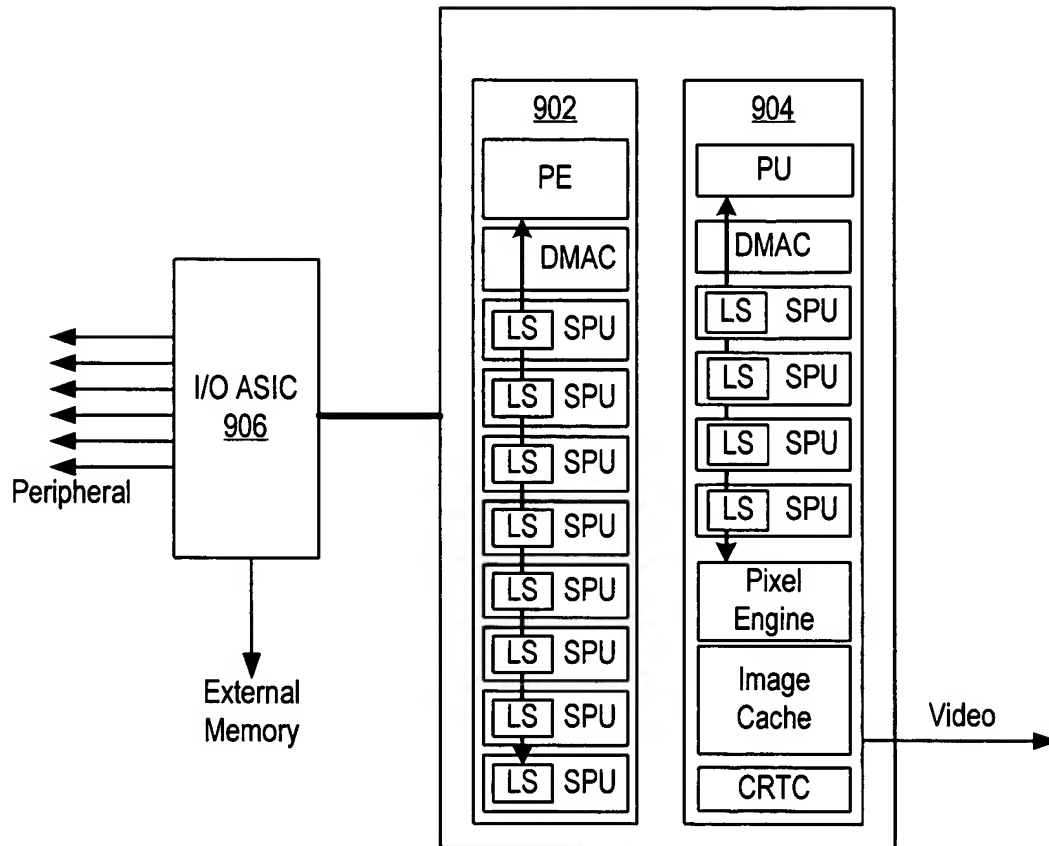
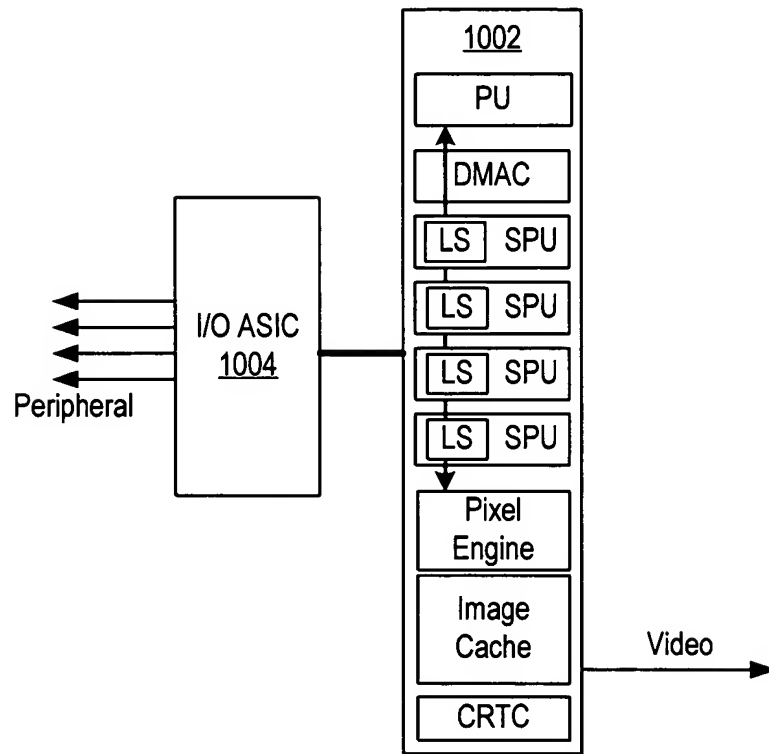
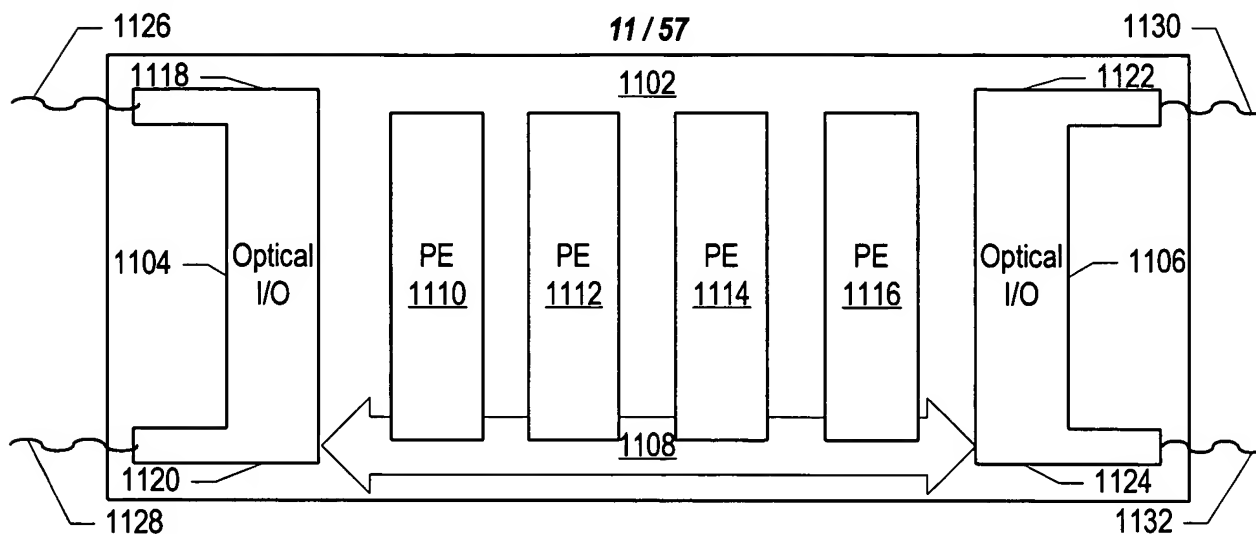
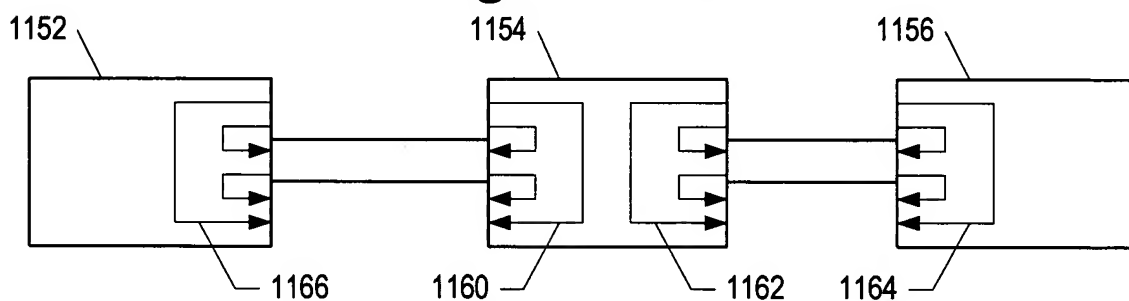
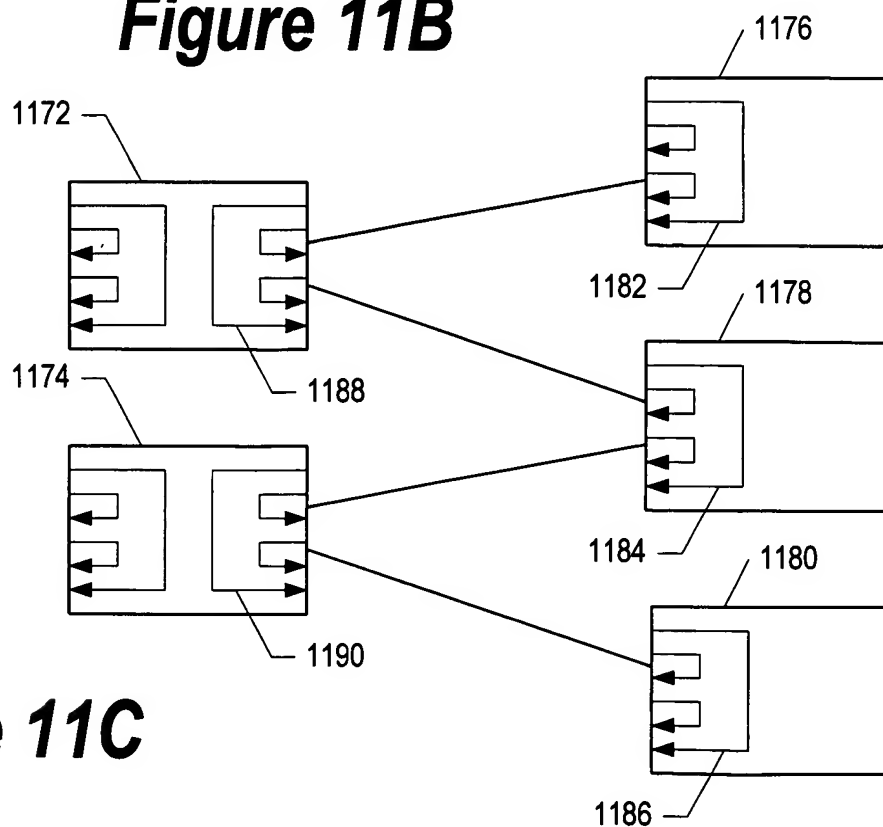


Figure 9

**Figure 10**

**Figure 11A****Figure 11B****Figure 11C**

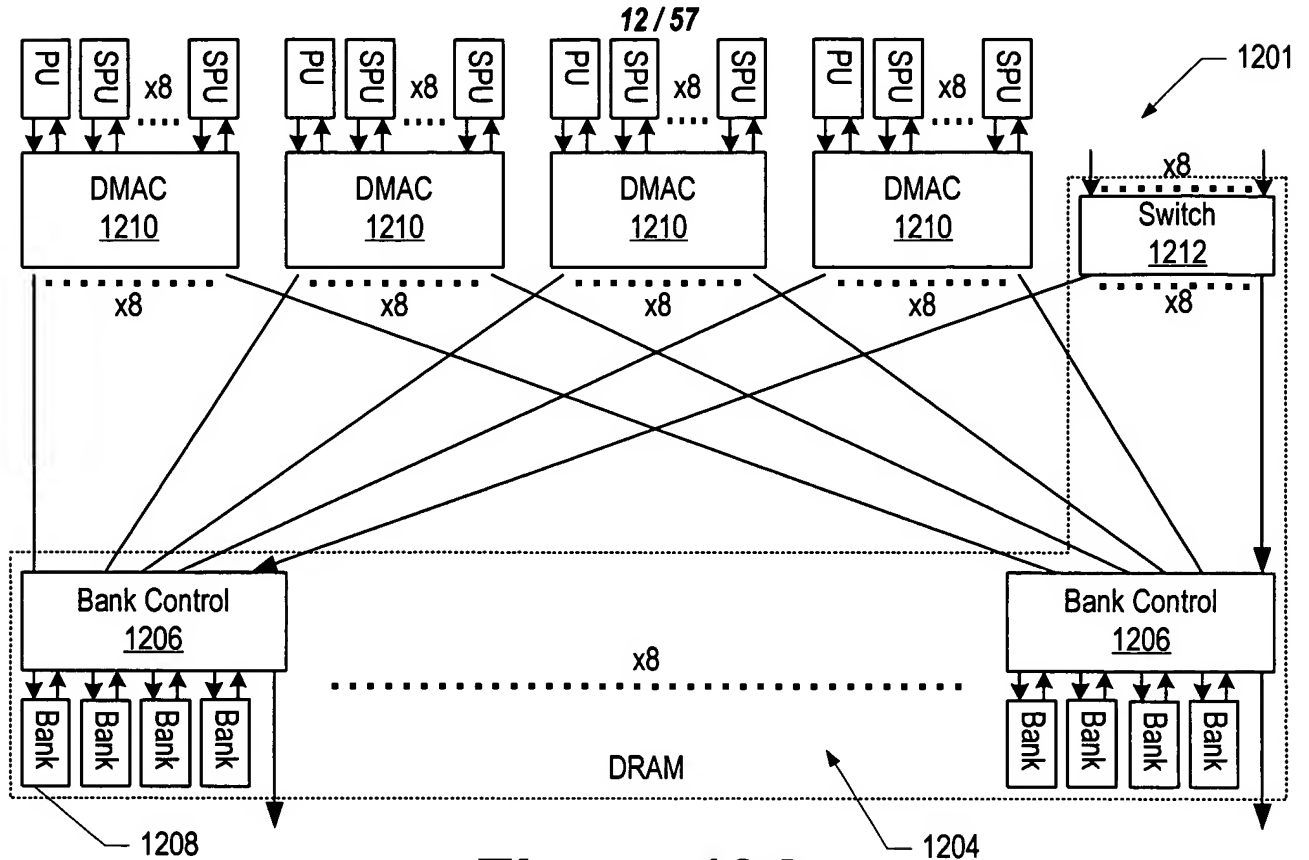


Figure 12A

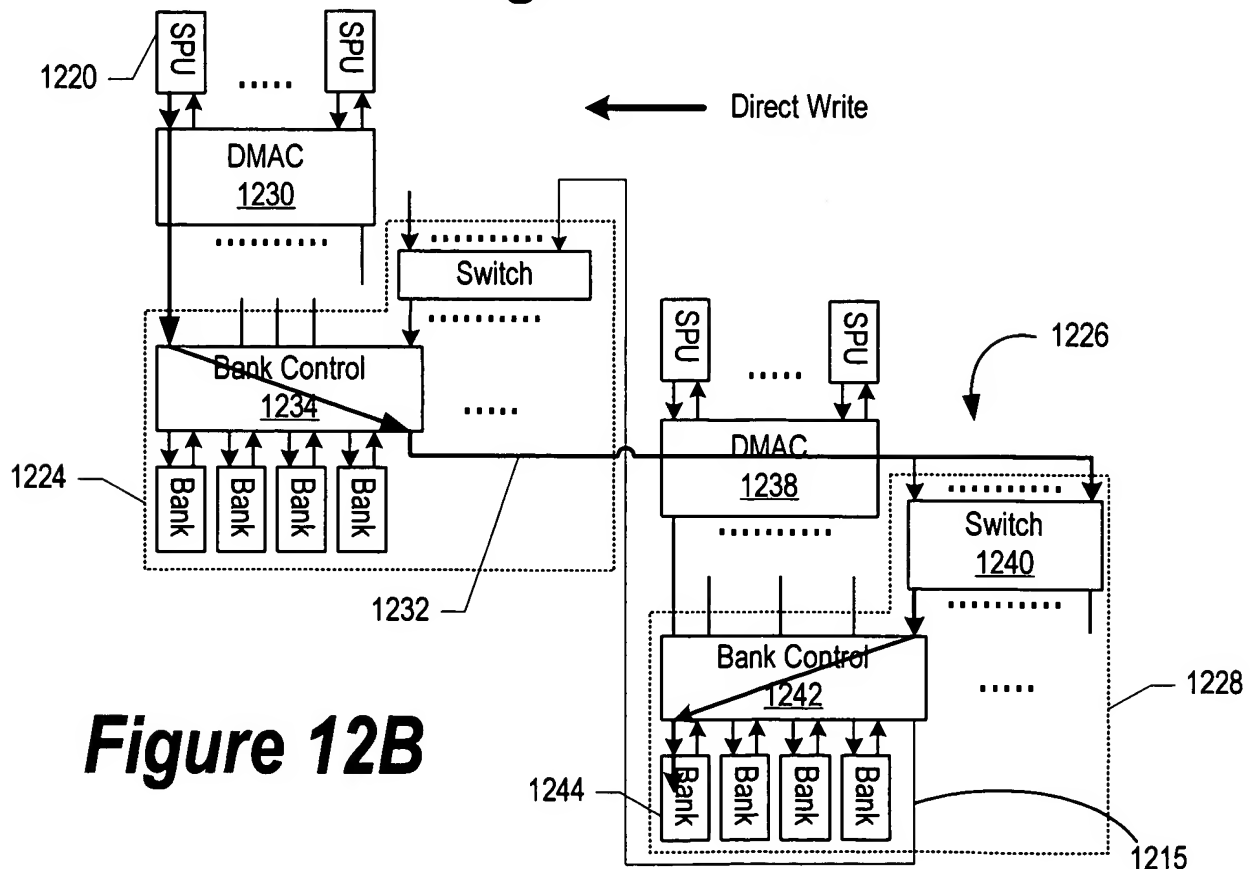


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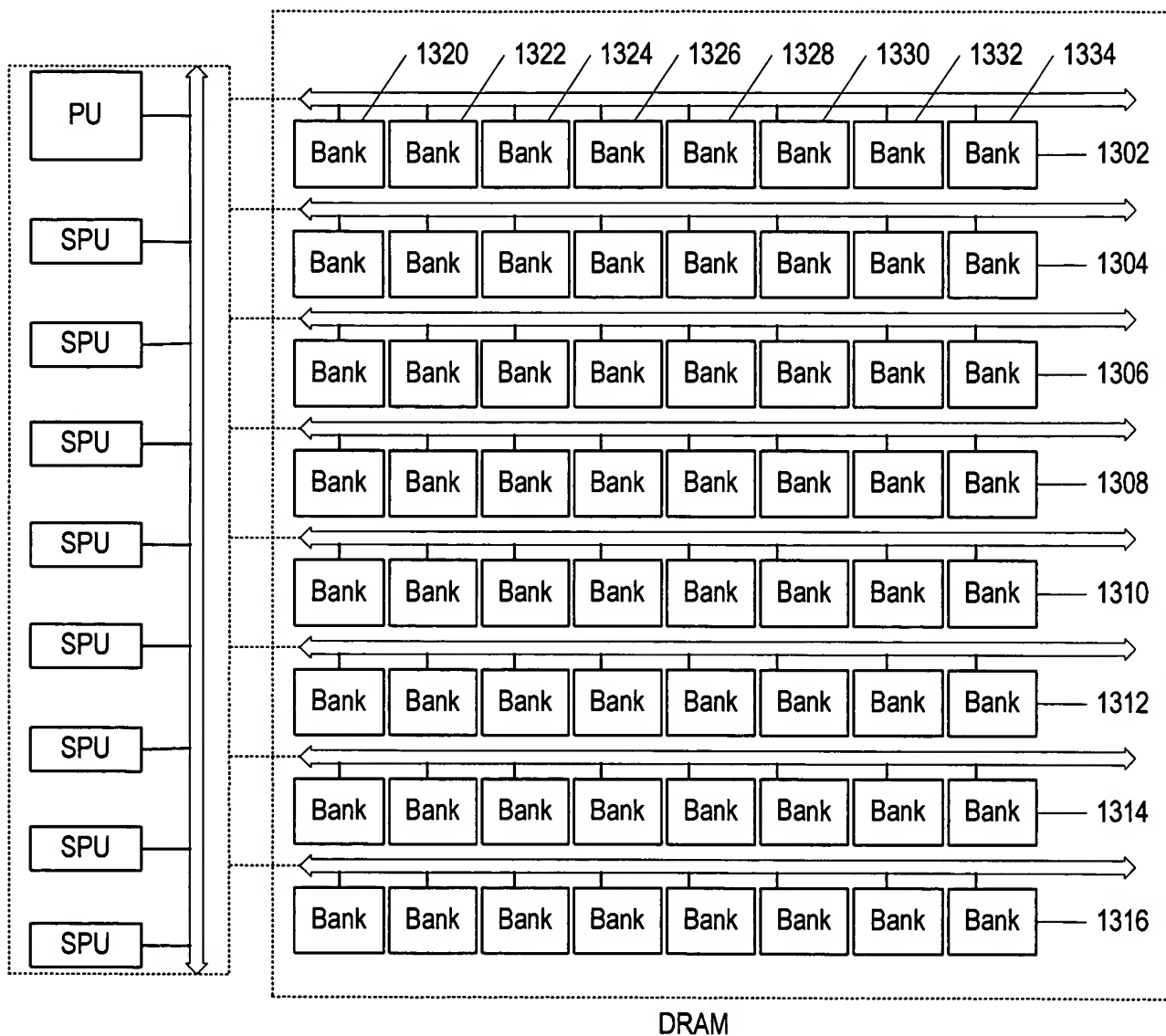
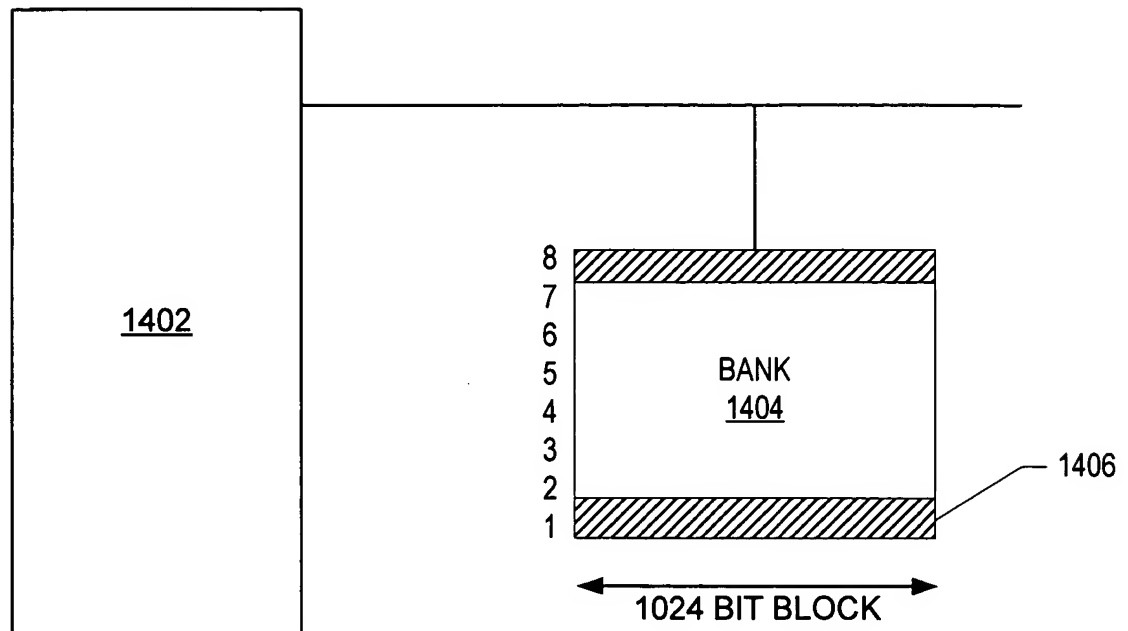
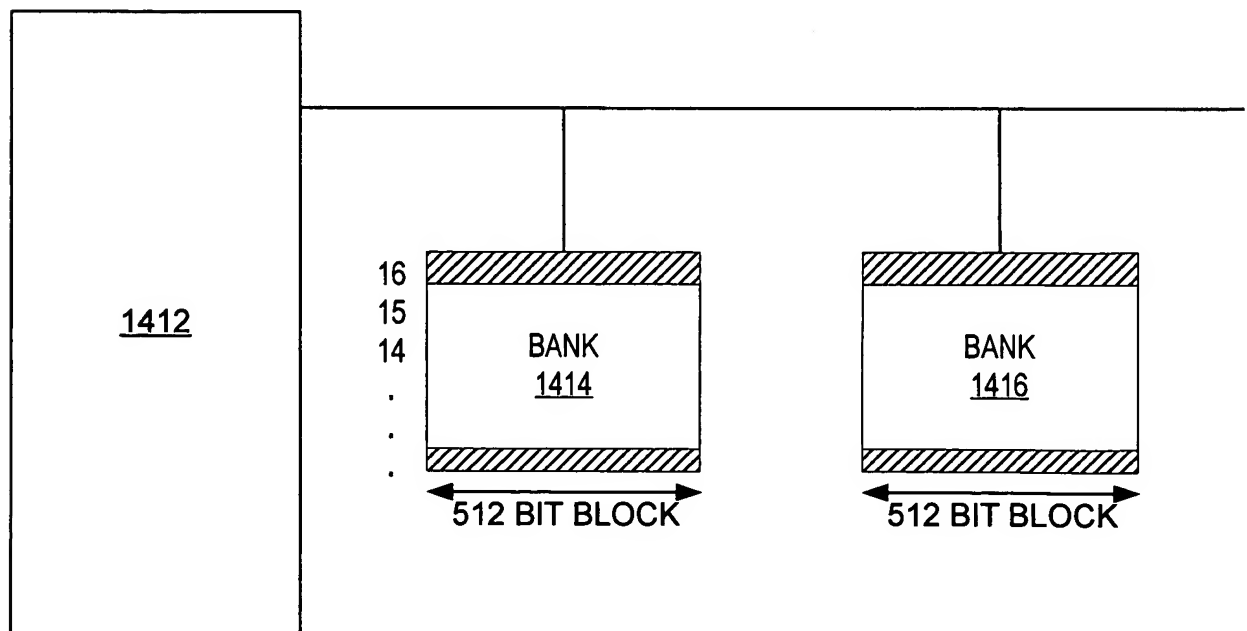


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**Figure 14A****Figure 14B**



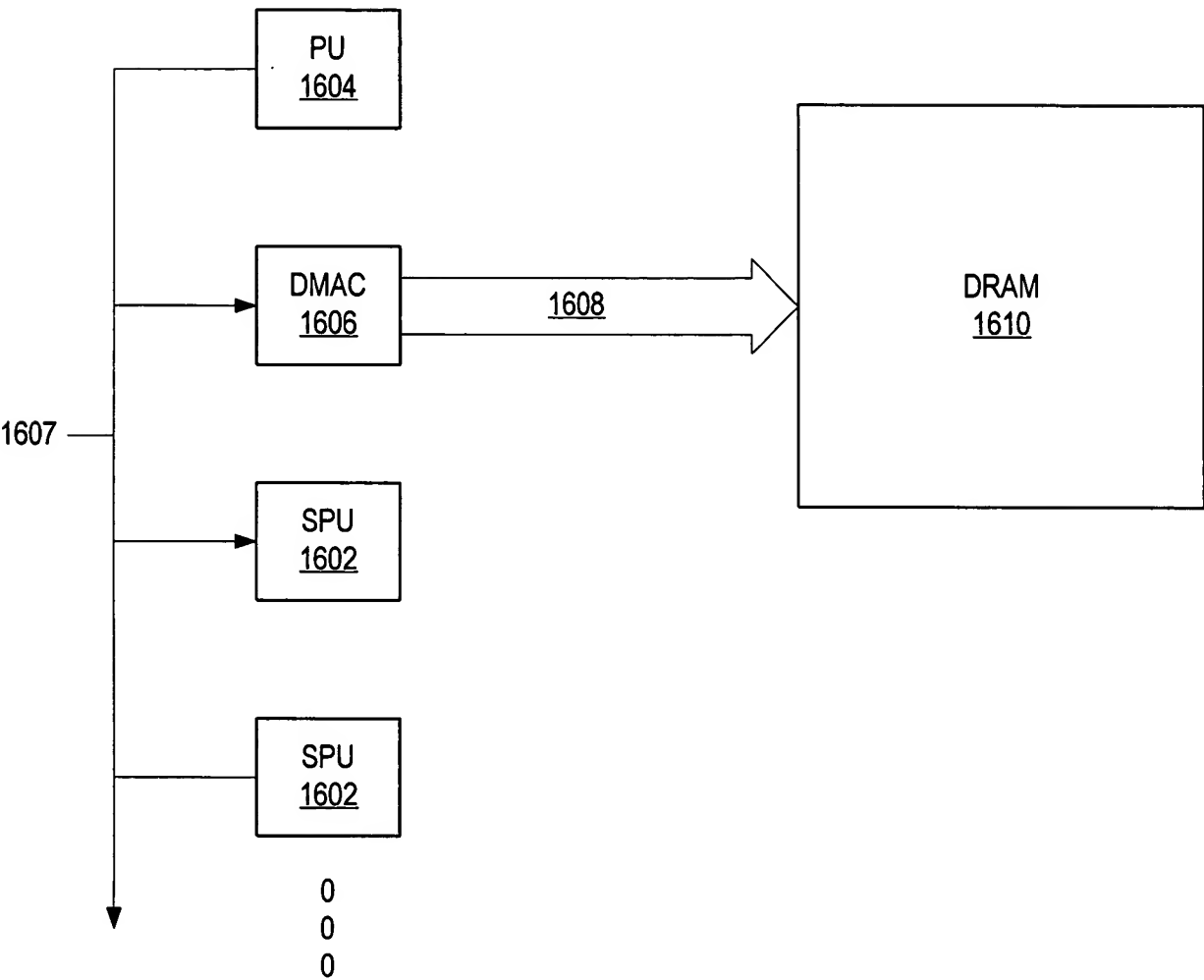


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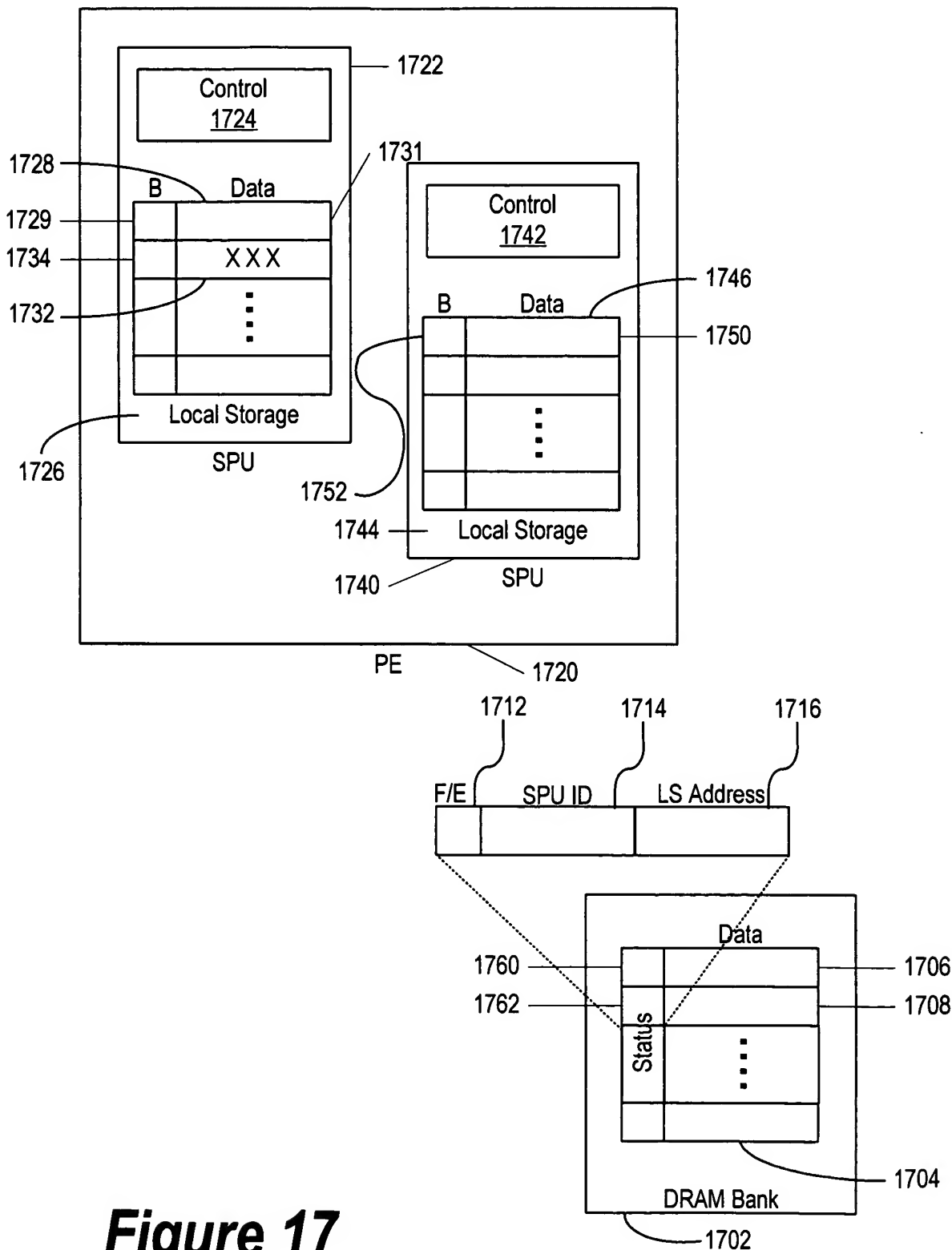
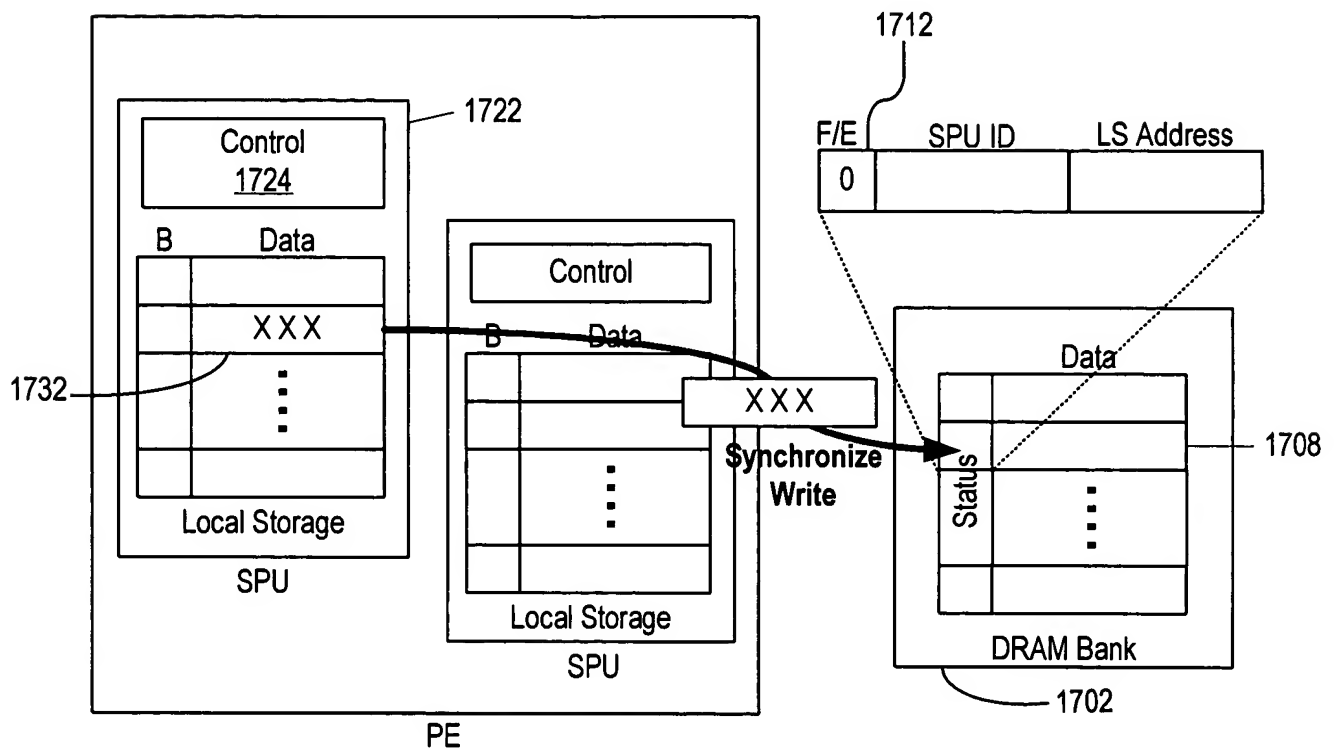


Figure 17

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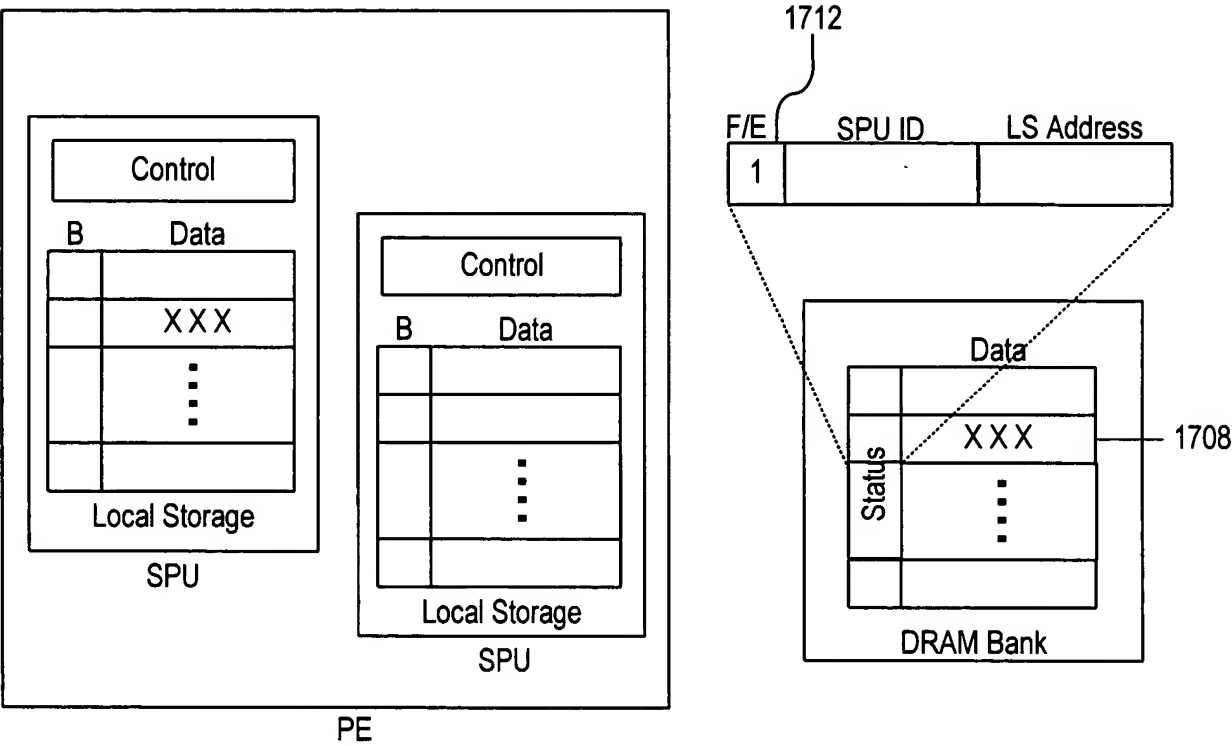


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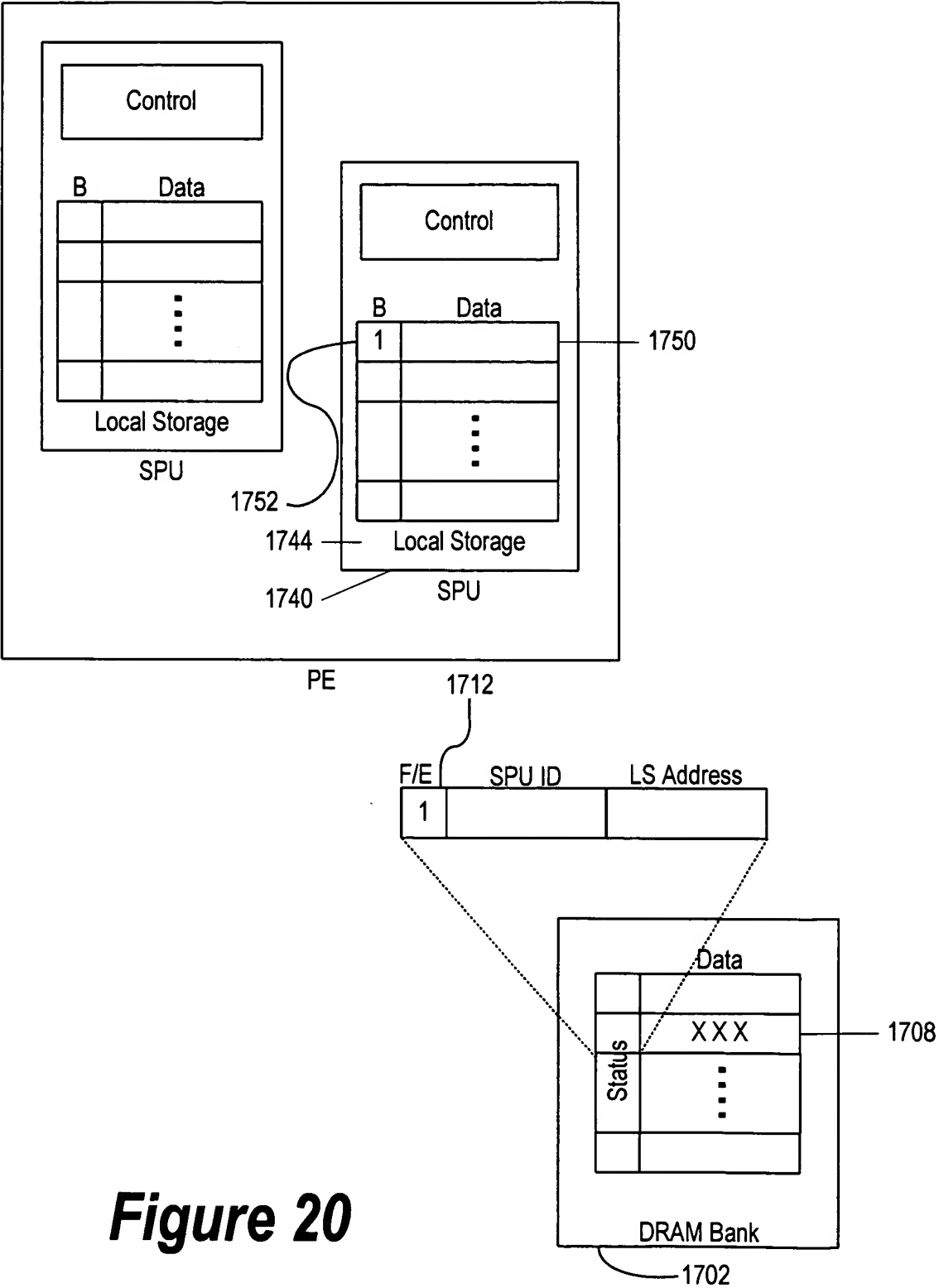


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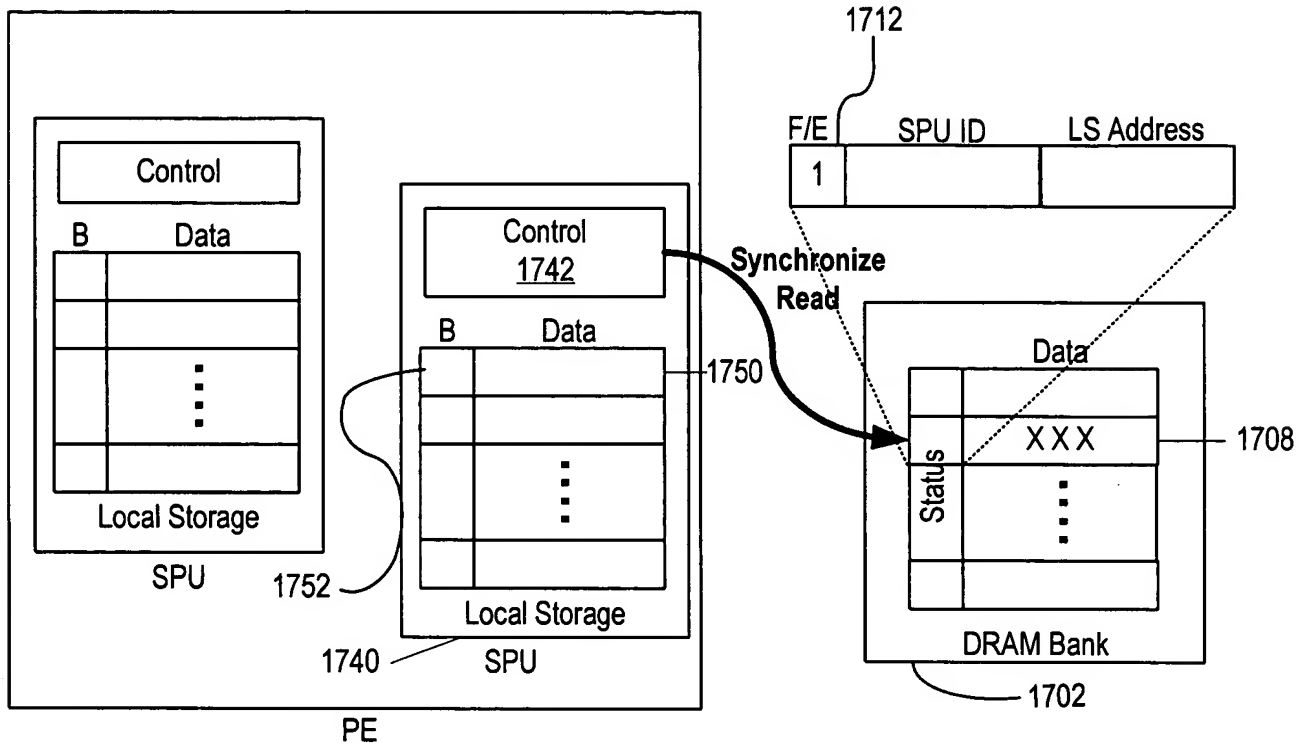
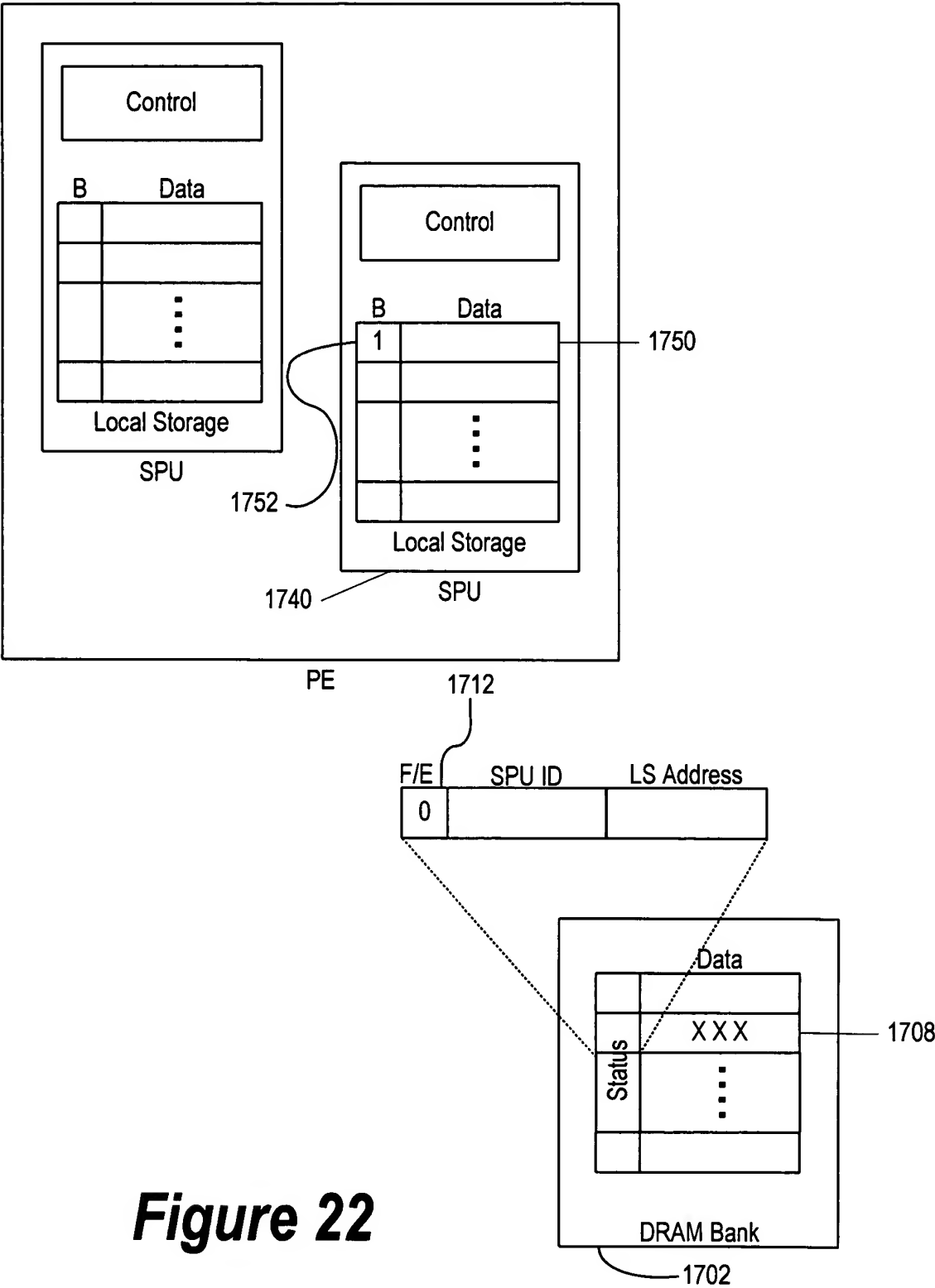


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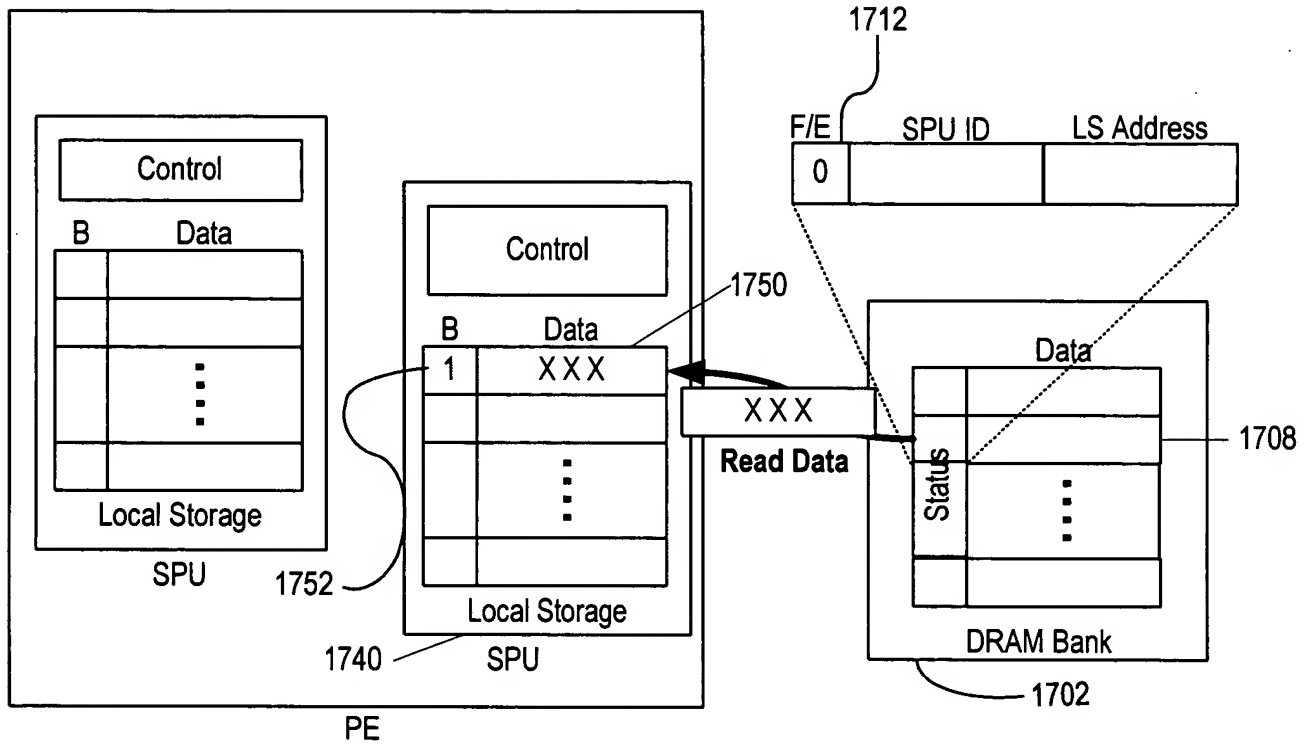
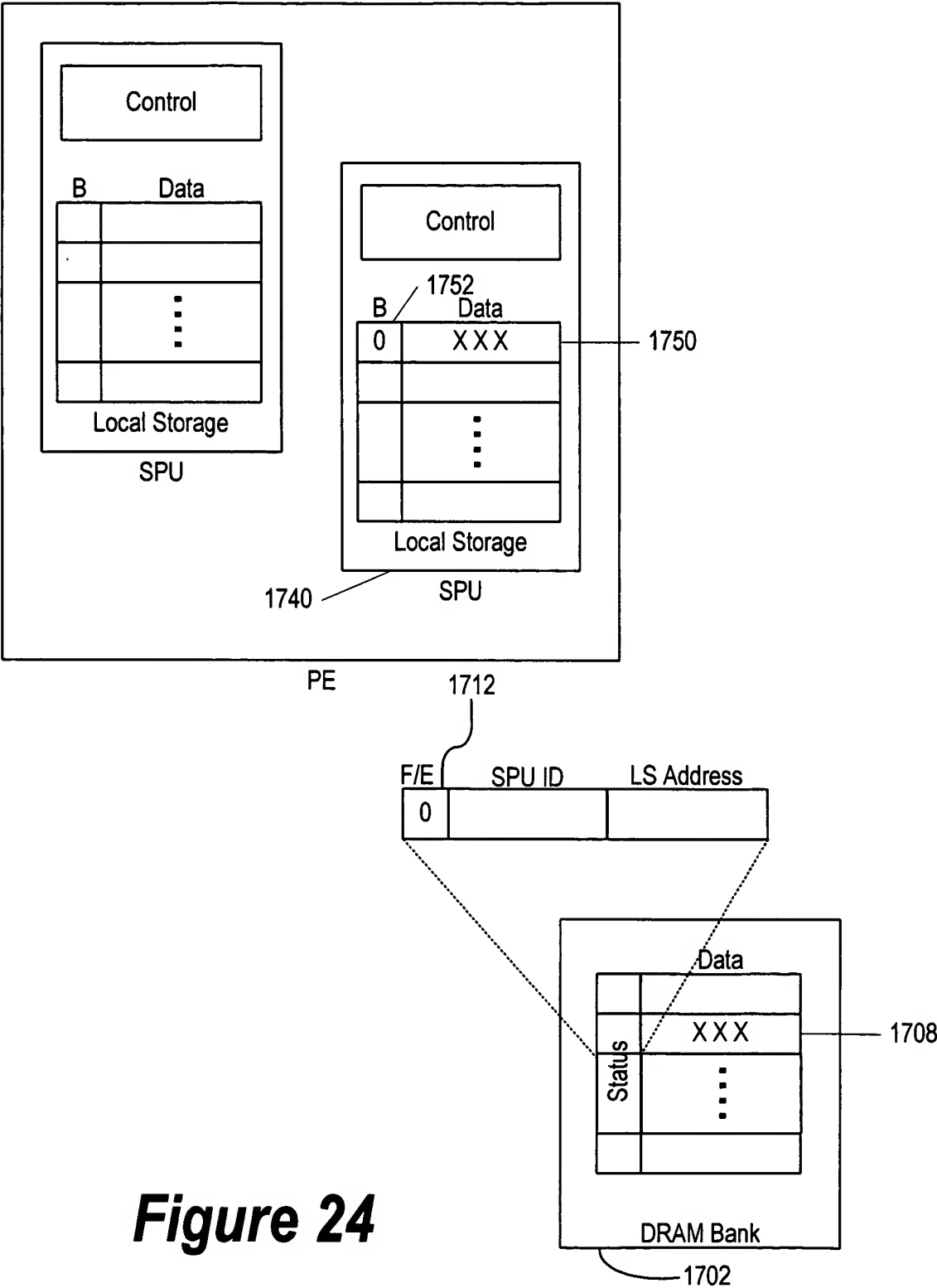
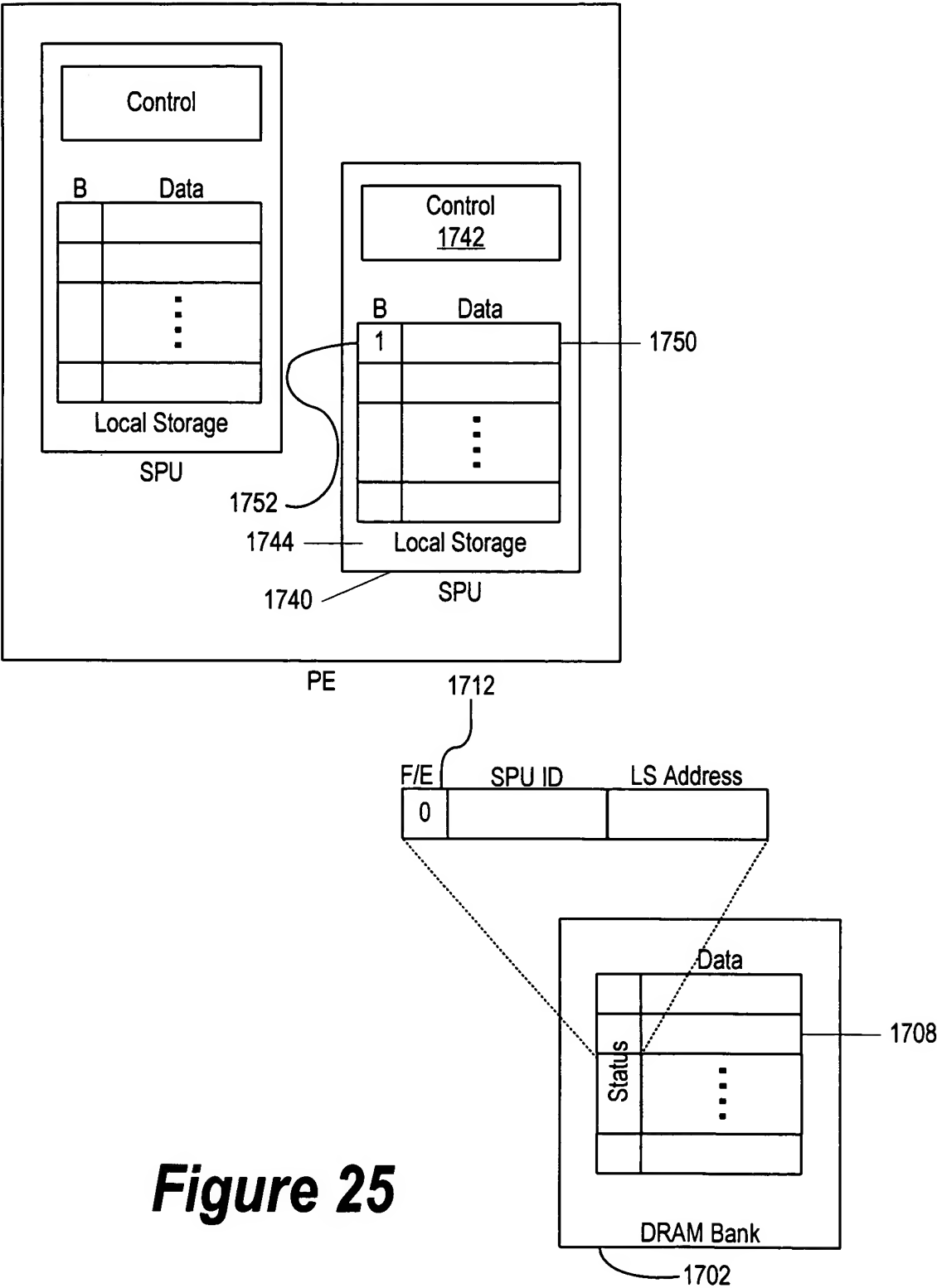


Figure 23





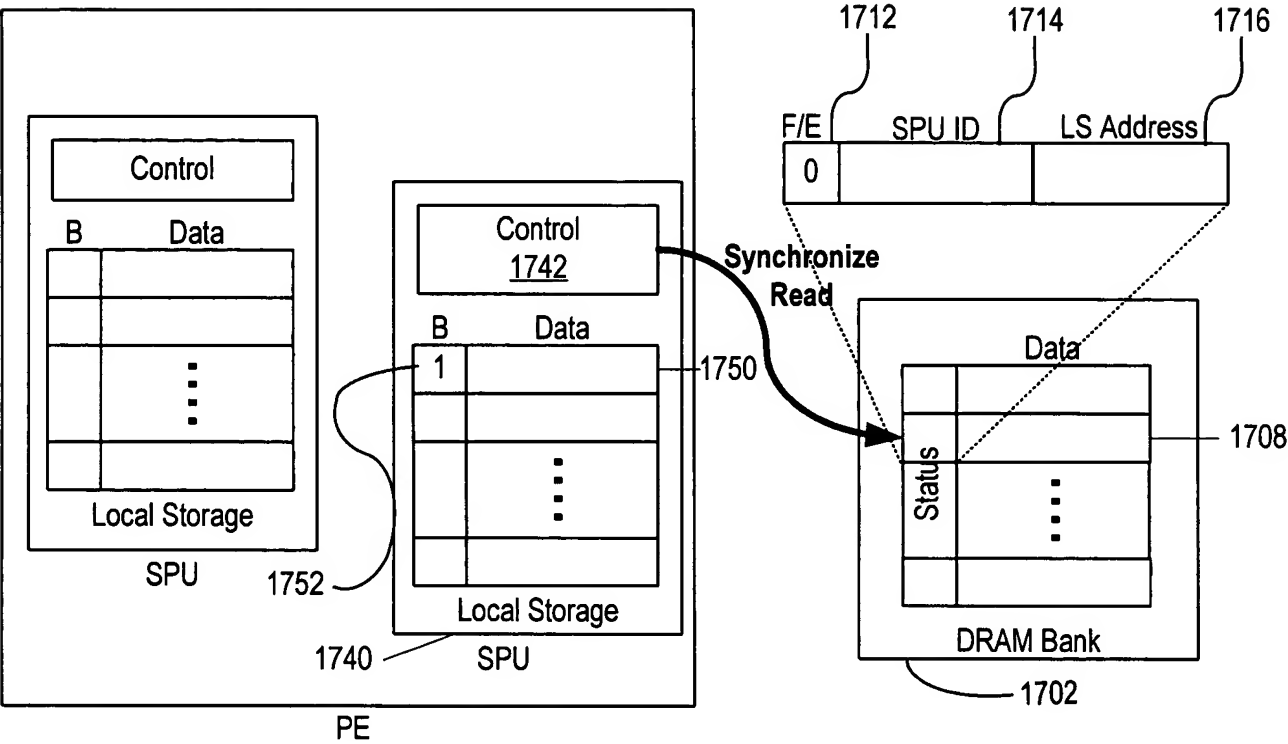


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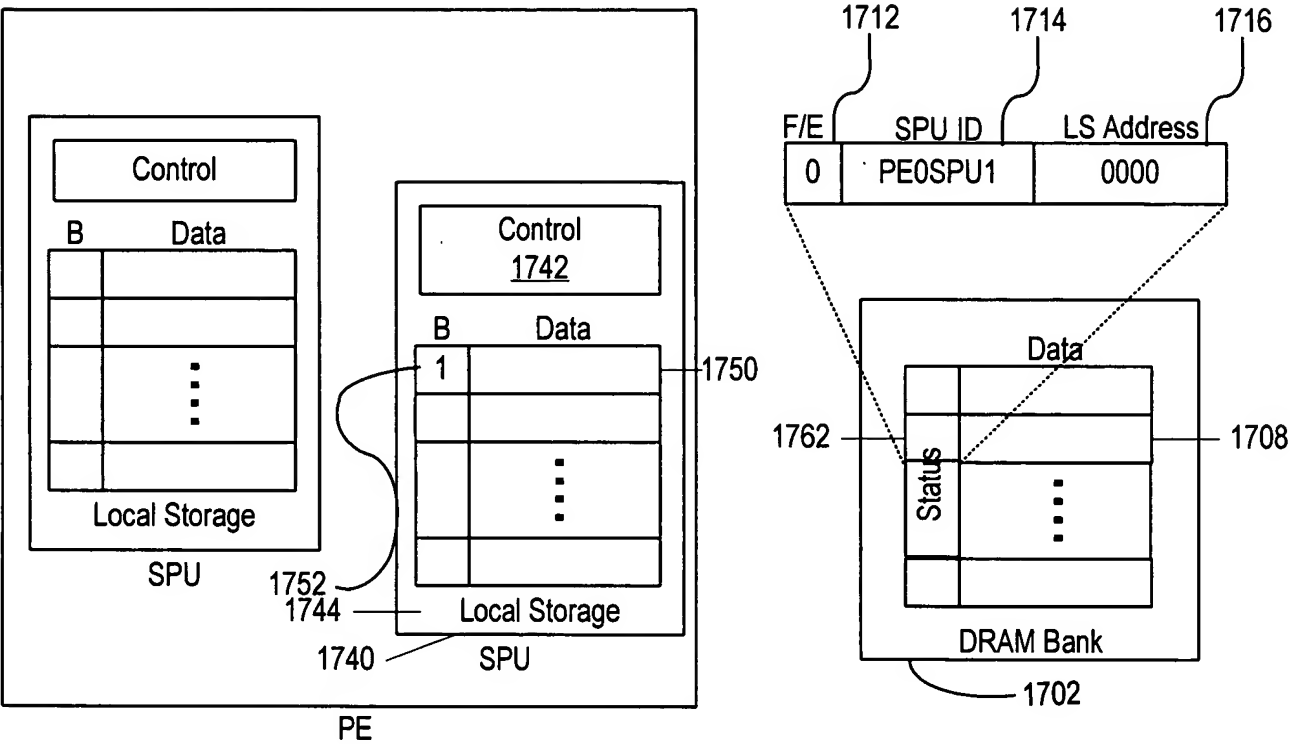


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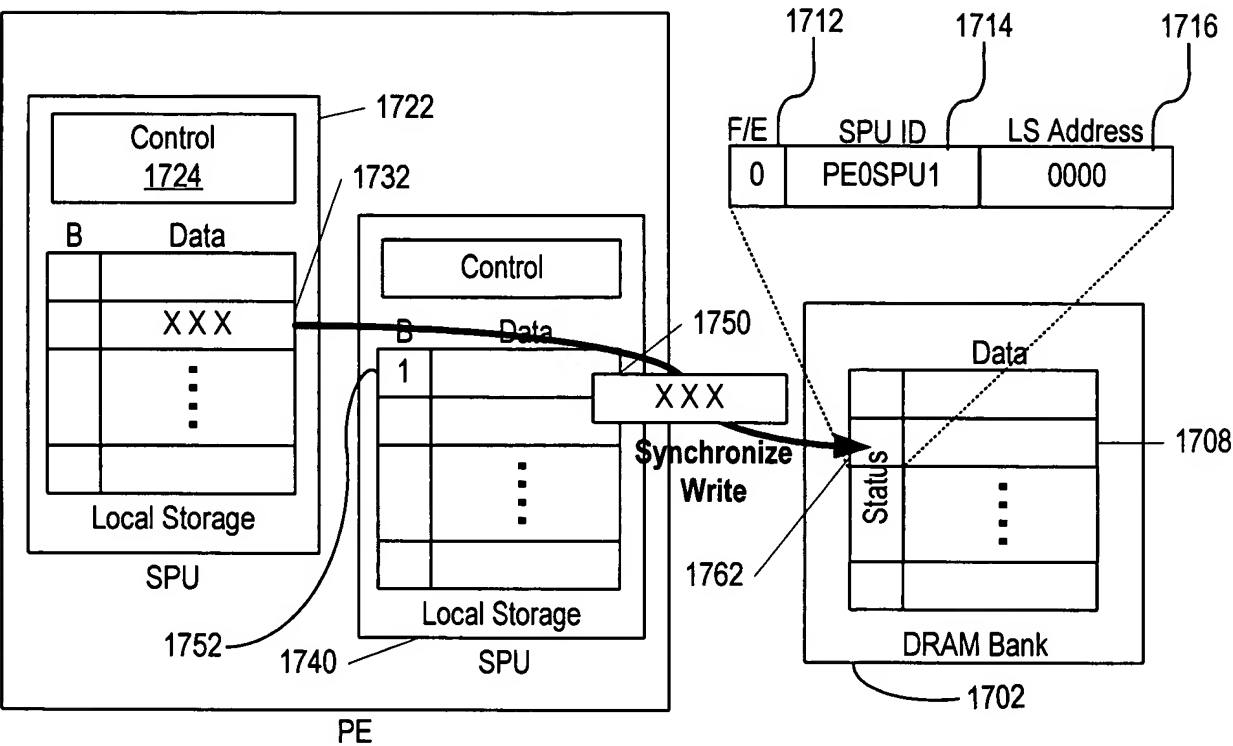


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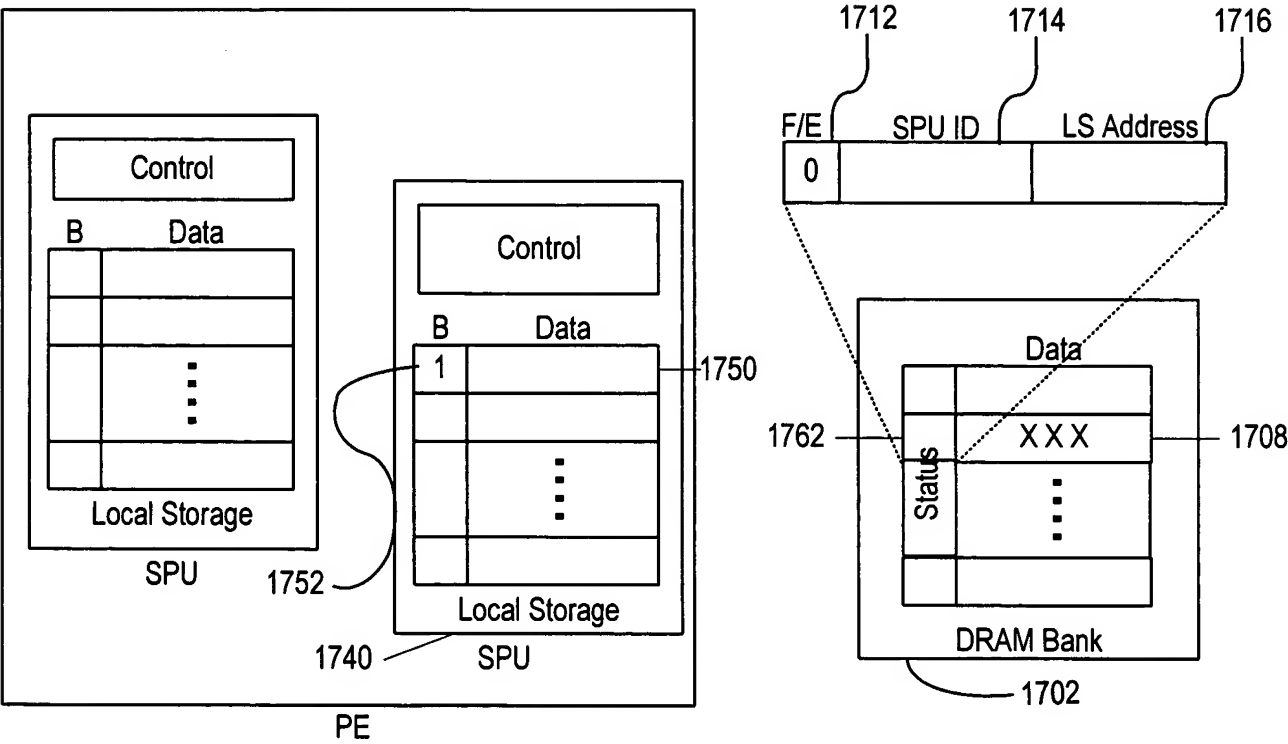


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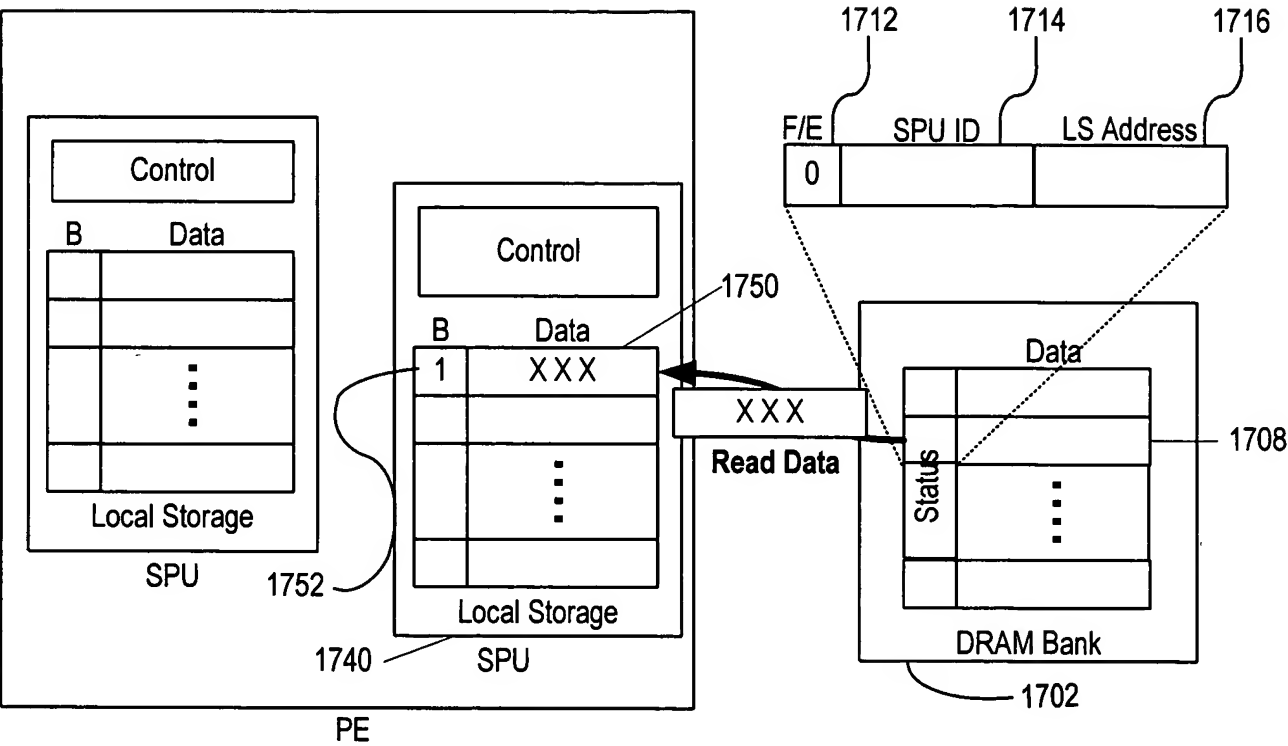
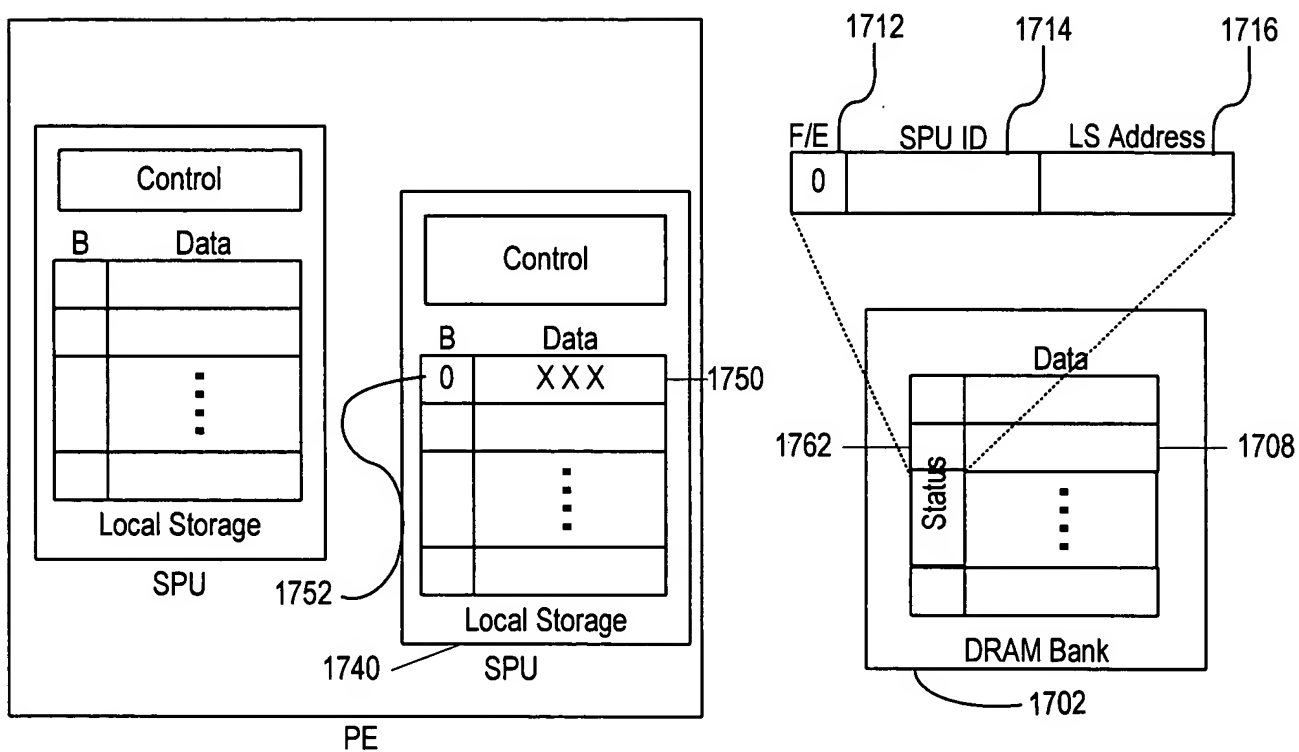
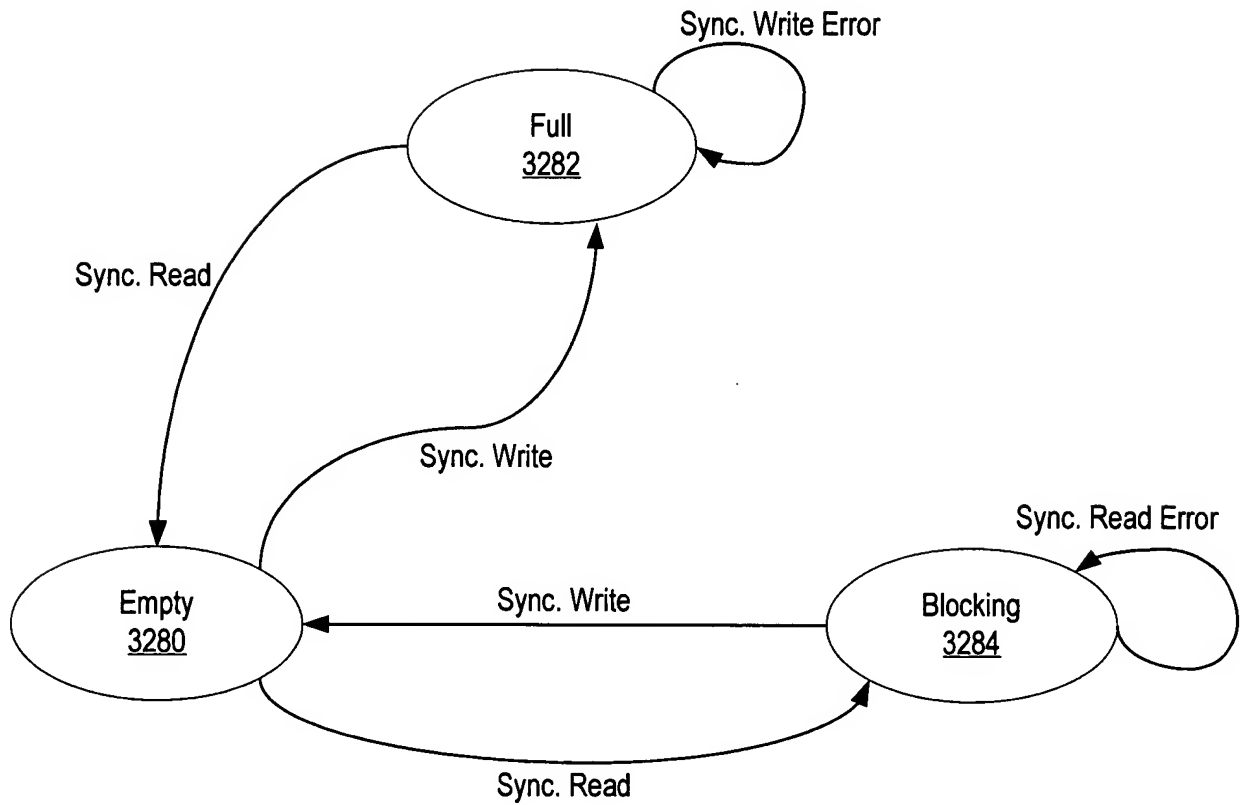


Figure 30

**Figure 31**

**Figure 32**

Key Control Table

3302

3304 ID 3306 3308

0	SPU Key	Key Mask
1	SPU Key	Key Mask
2	SPU Key	Key Mask
		⋮
7	SPU Key	Key Mask

Figure 33

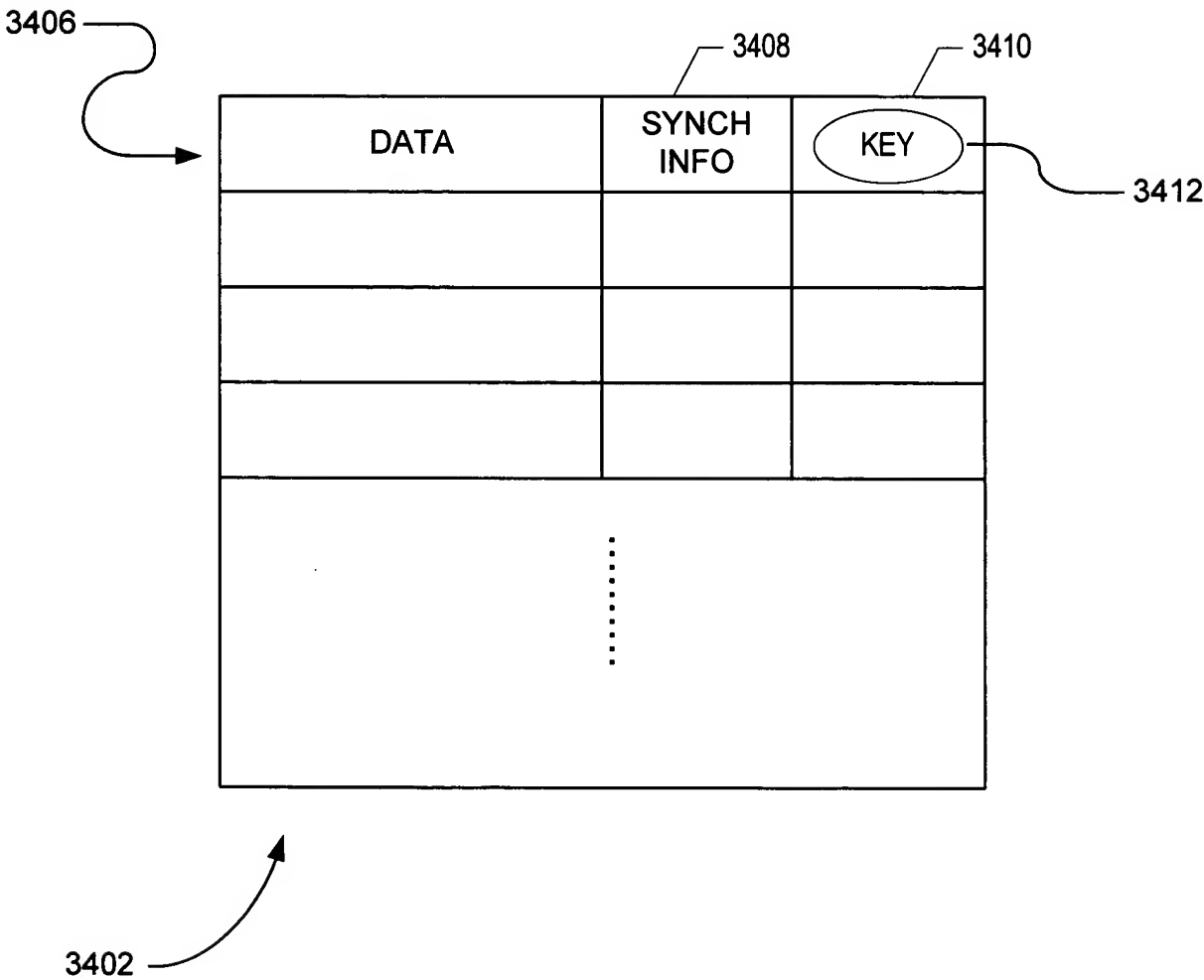


Figure 34

Memory Access Control Table

3504	ID	3506	3508	3510	3512
0	Base	Size	Access Key	Access Key Mask	
1	Base	Size	Access Key	Access Key Mask	
2	Base	Size	Access Key	Access Key Mask	
63	Base	Size	Access Key	Access Key Mask	

3502

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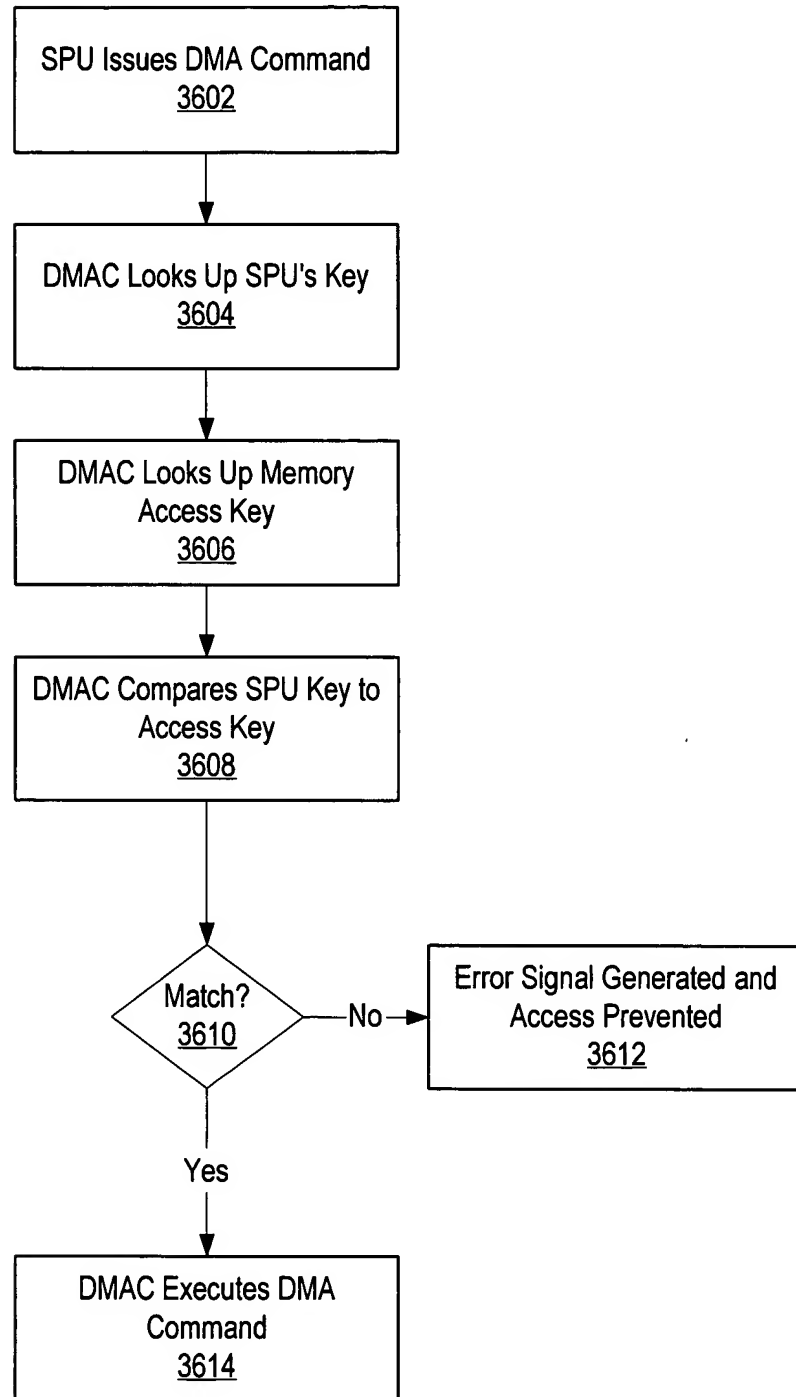


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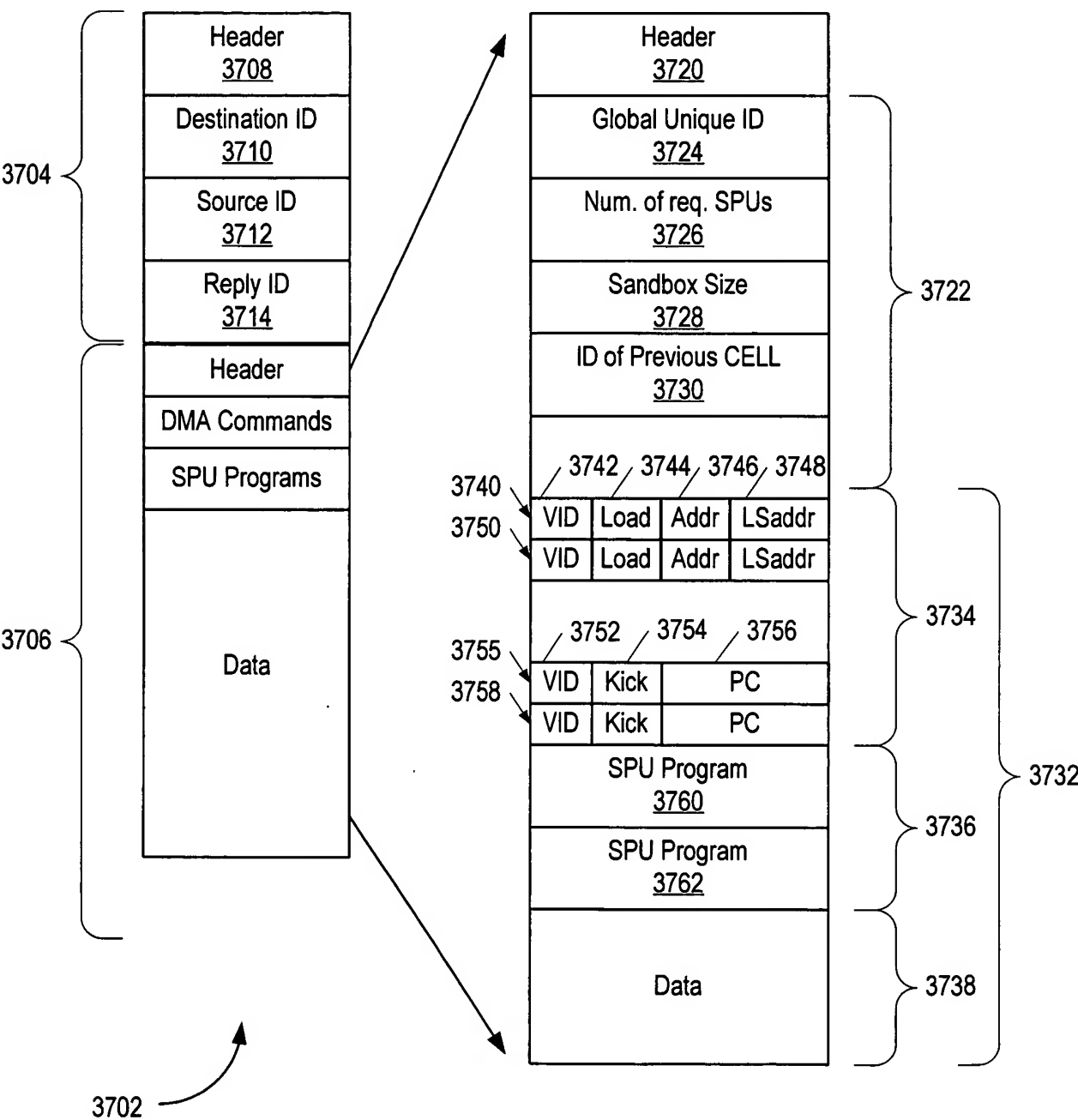


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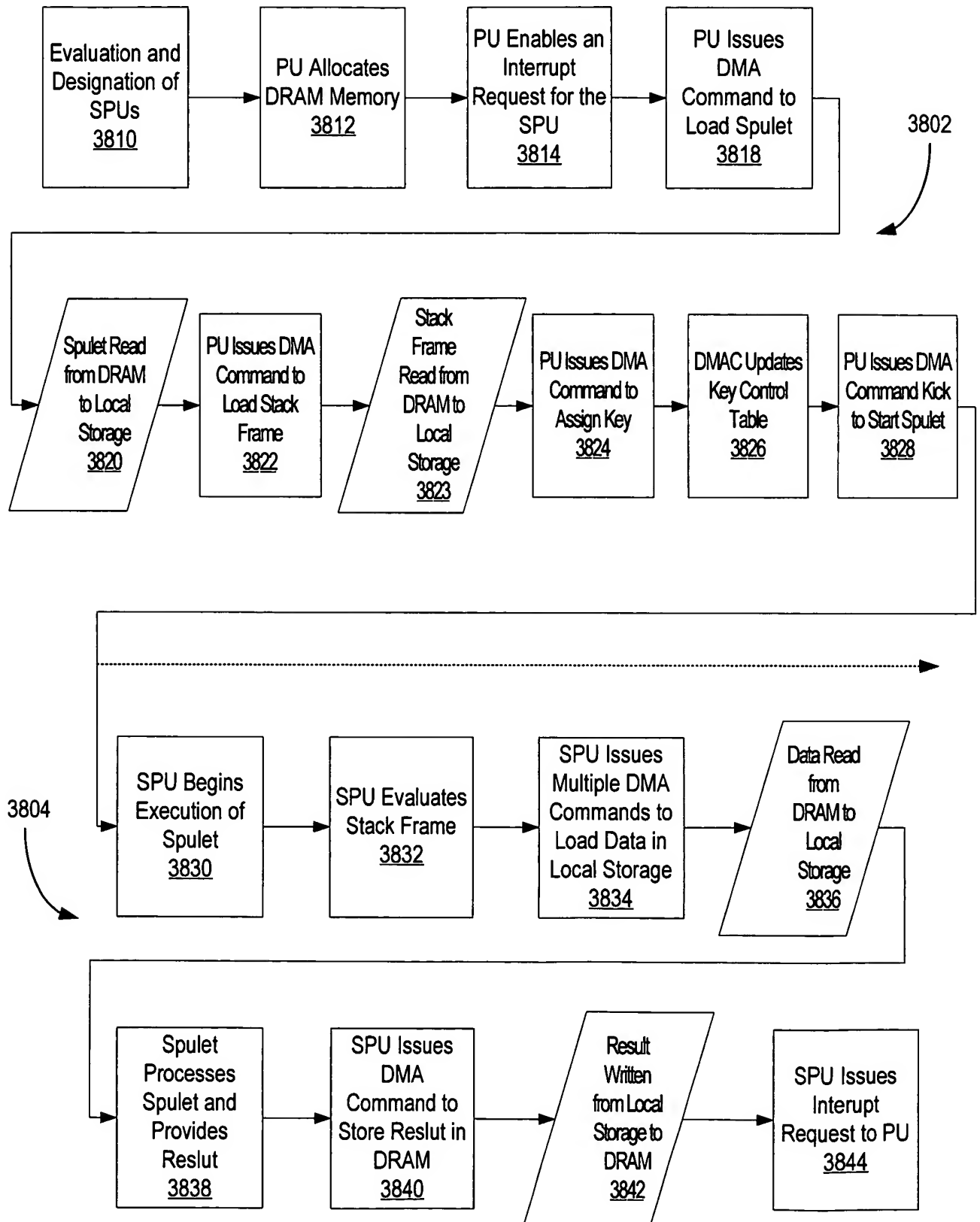


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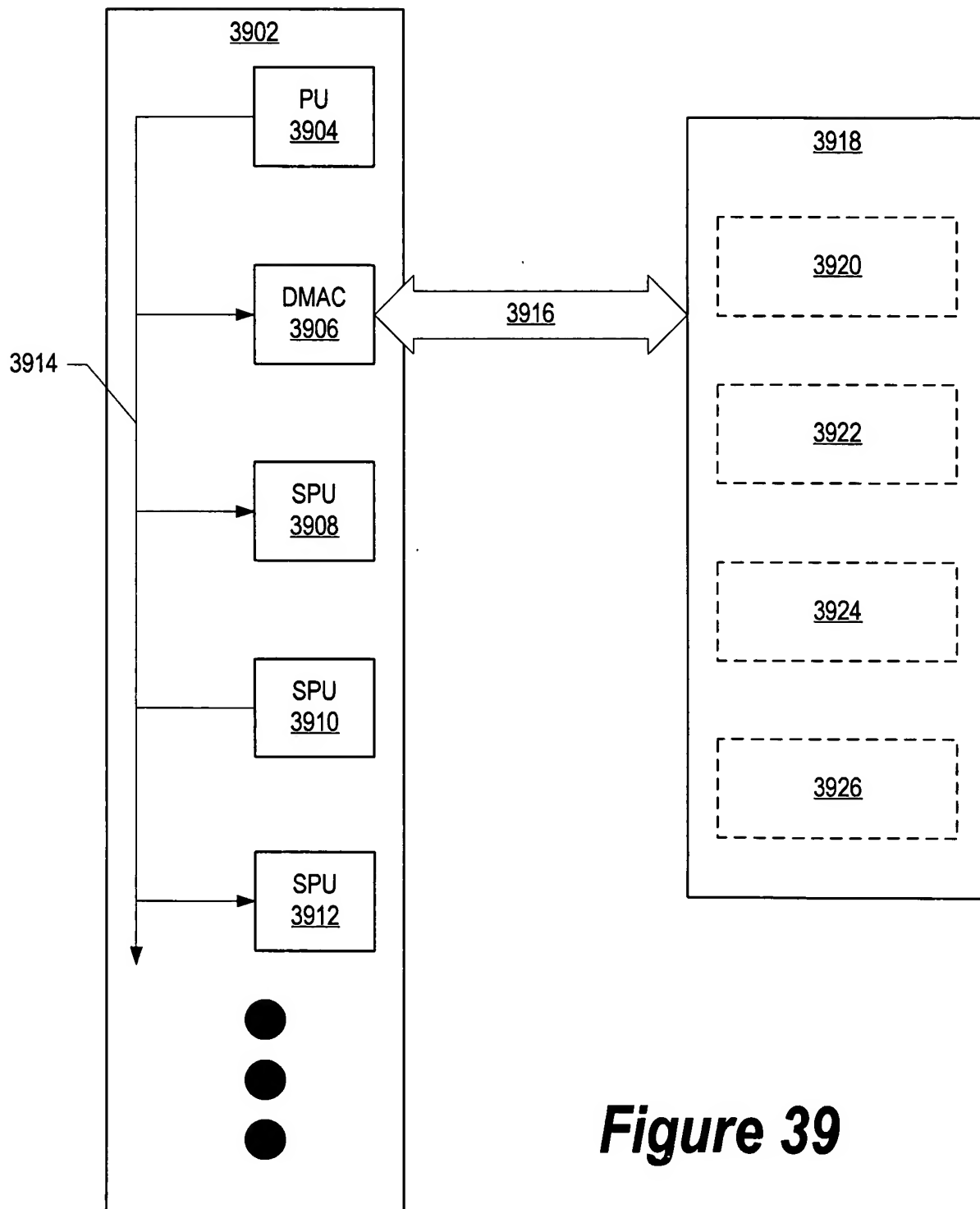


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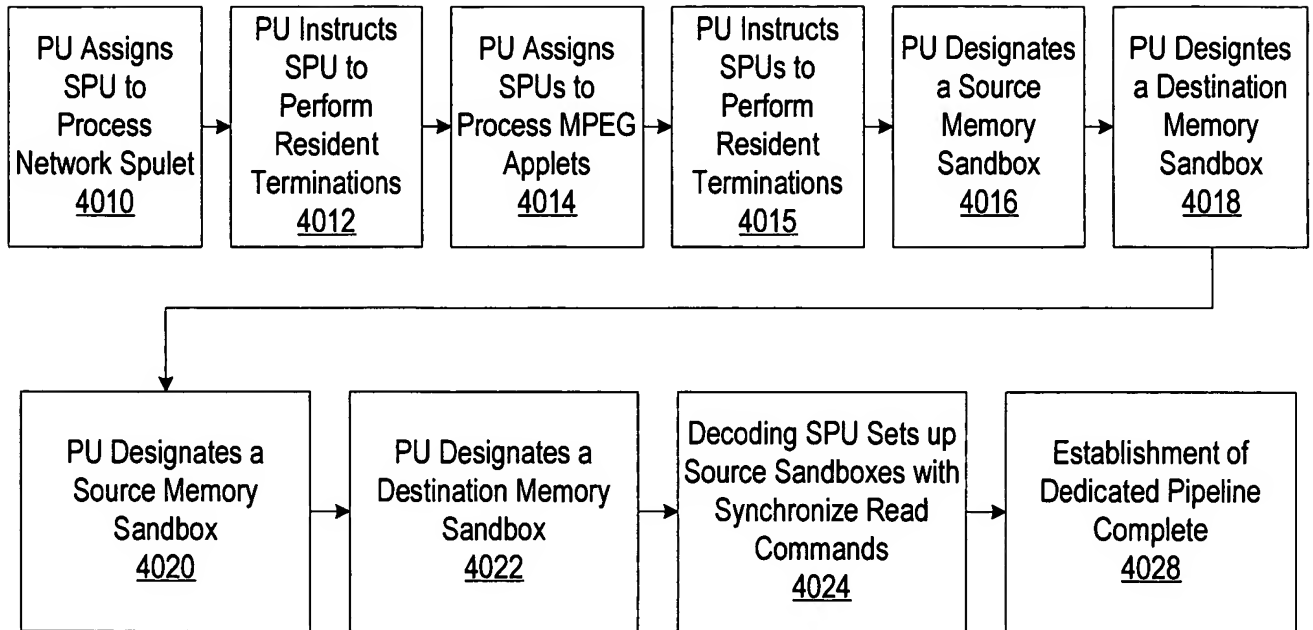


Figure 40A

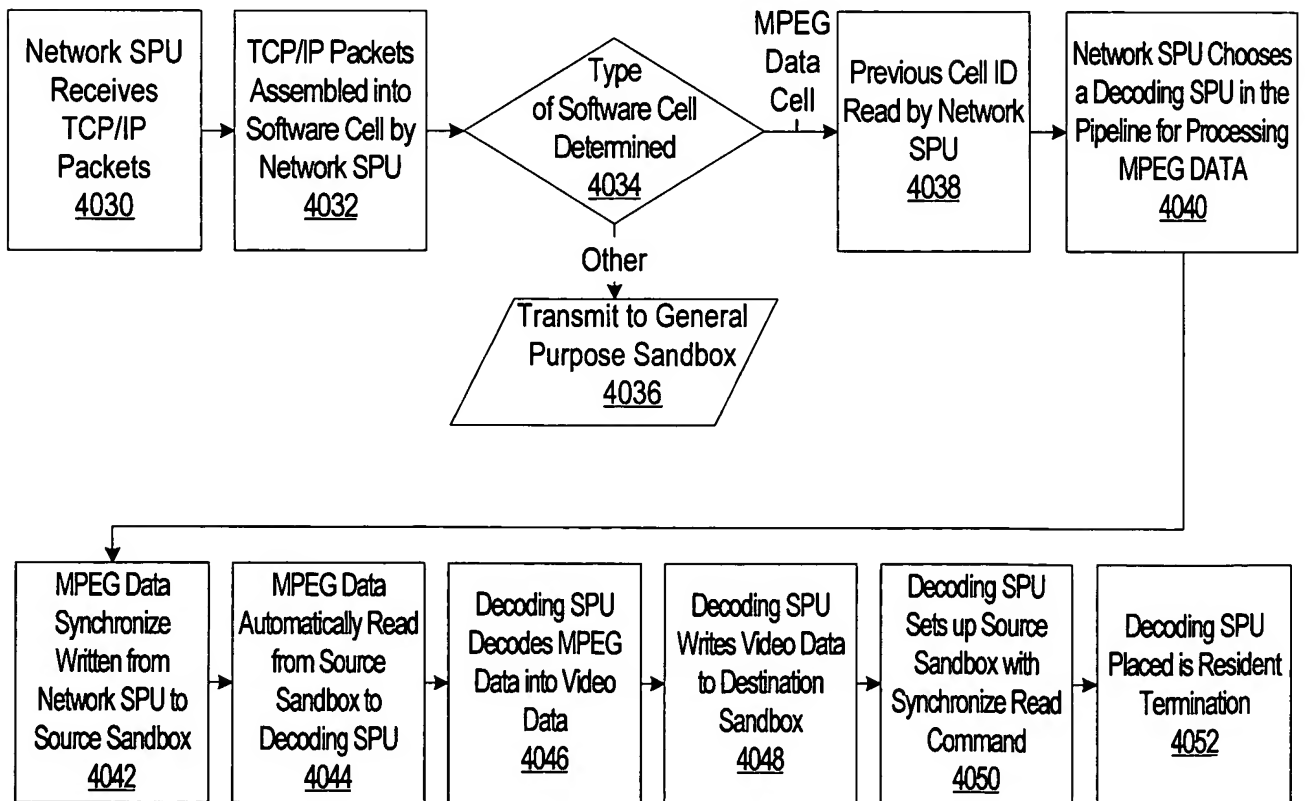


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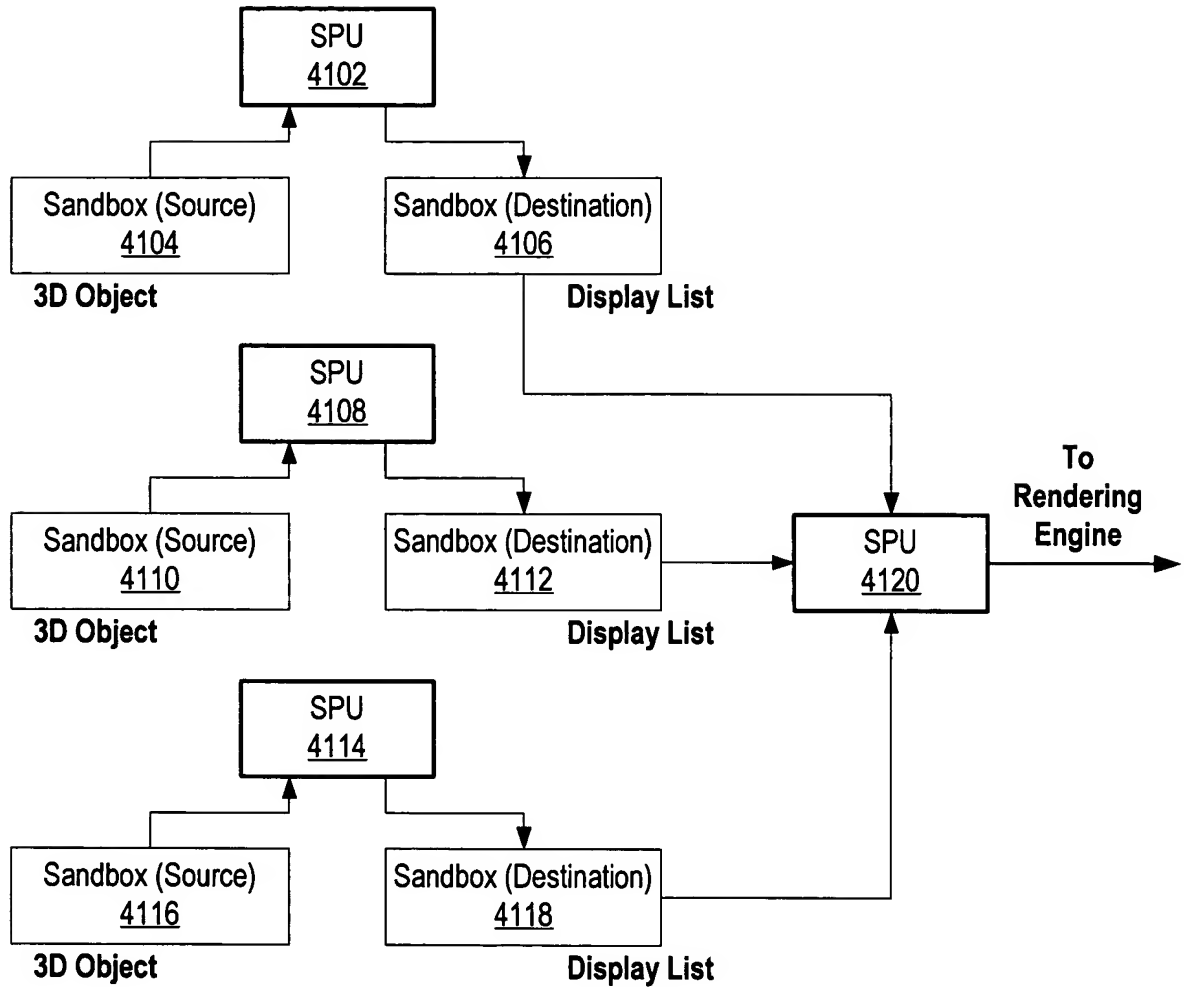


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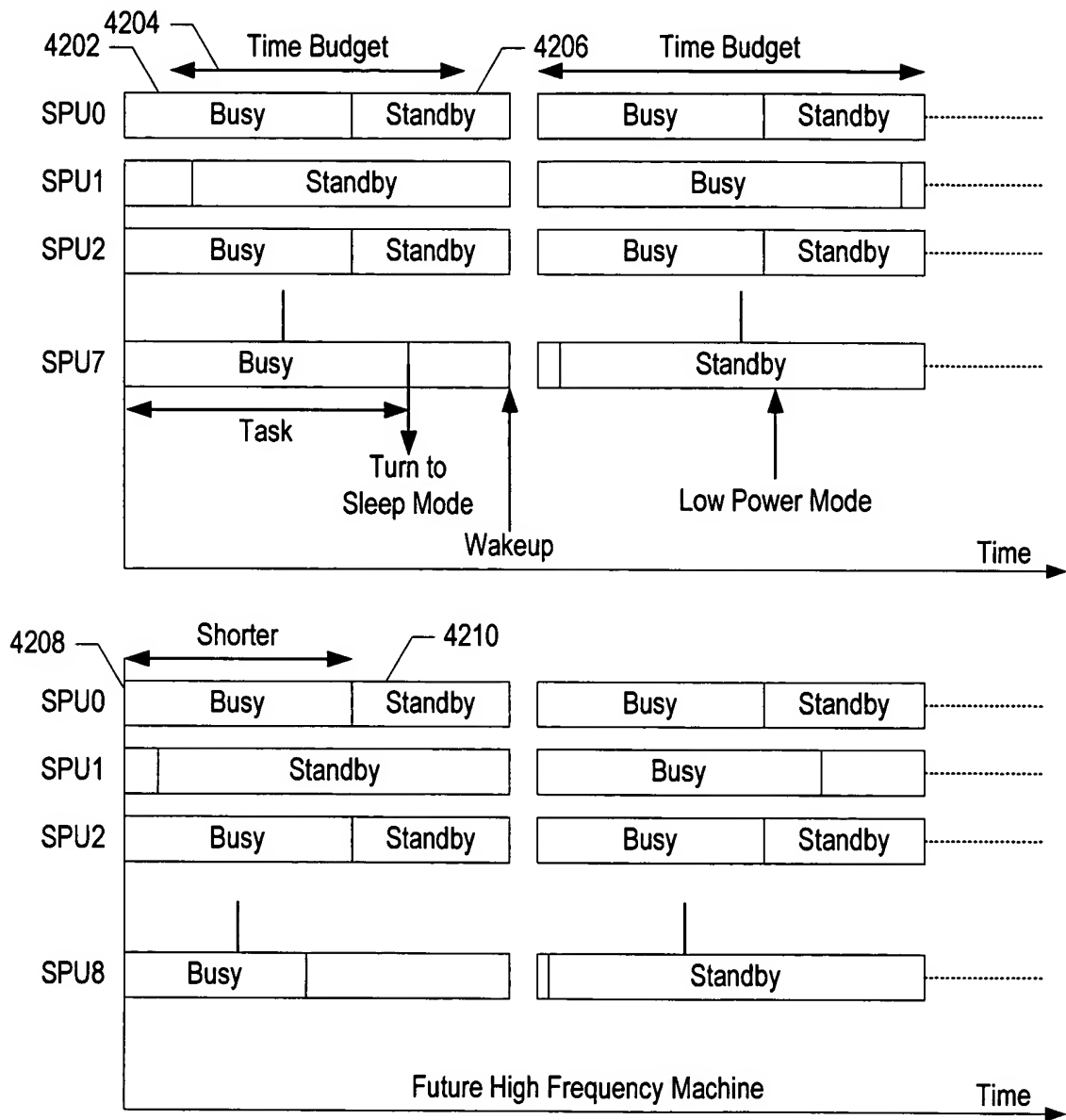


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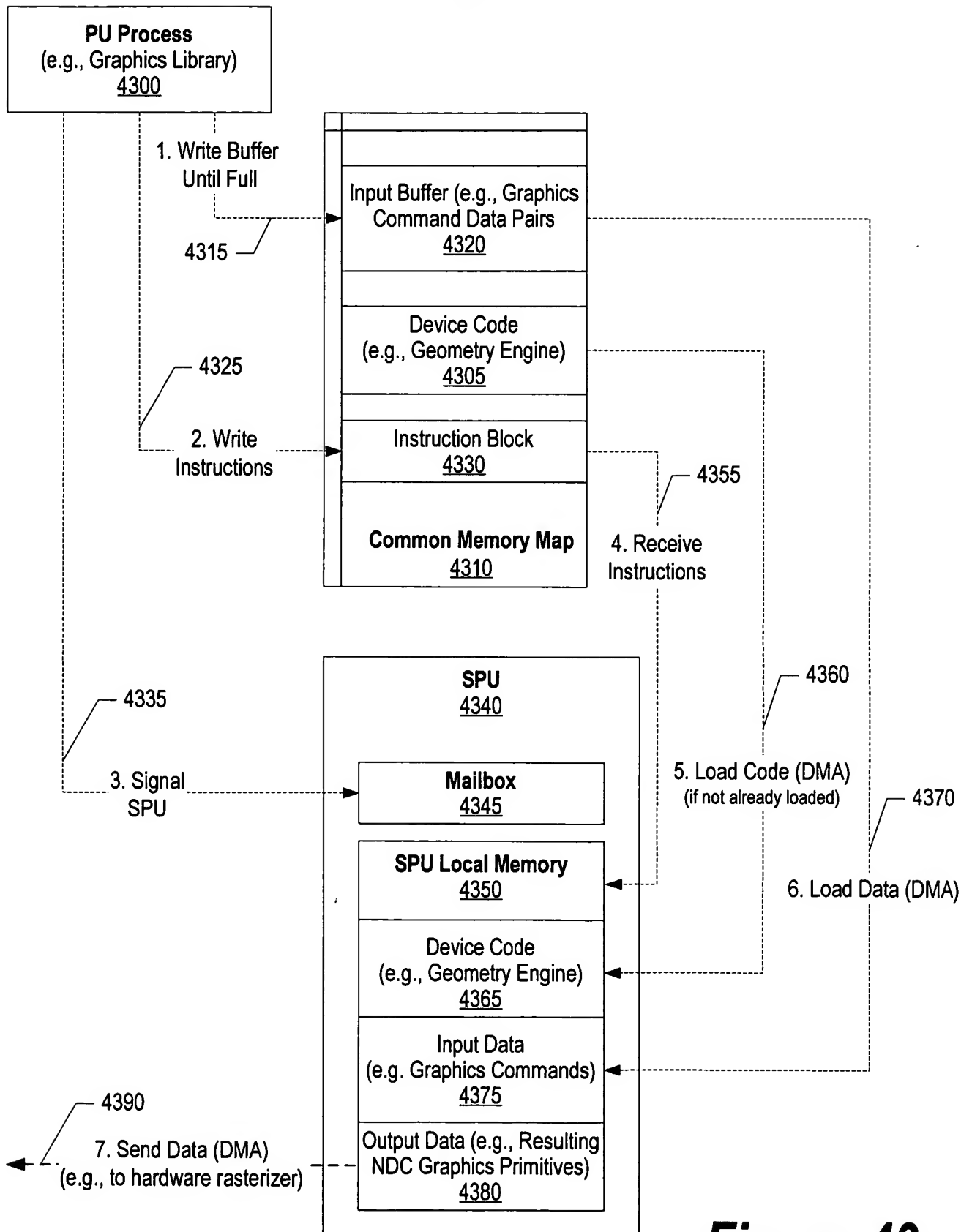


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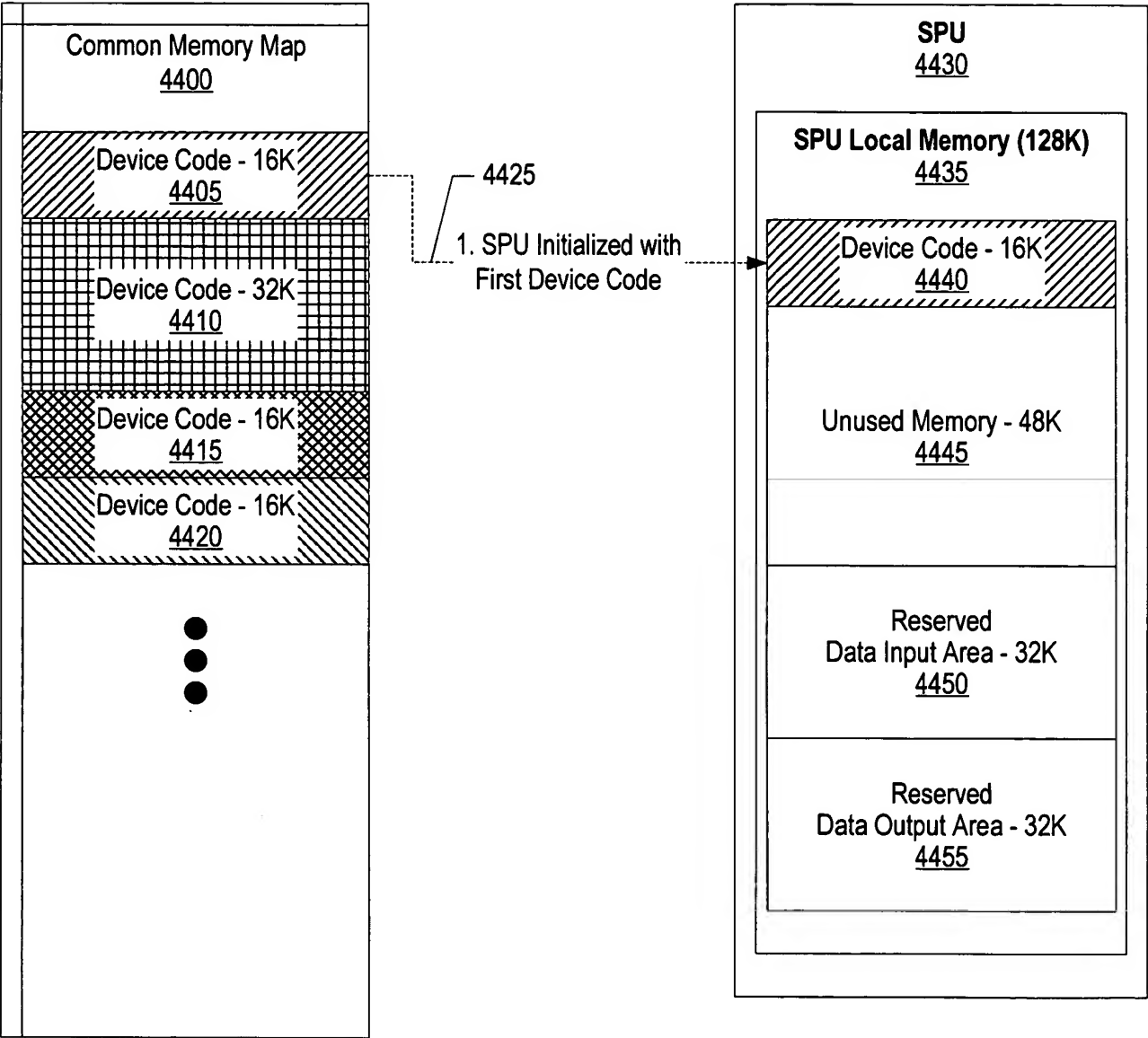


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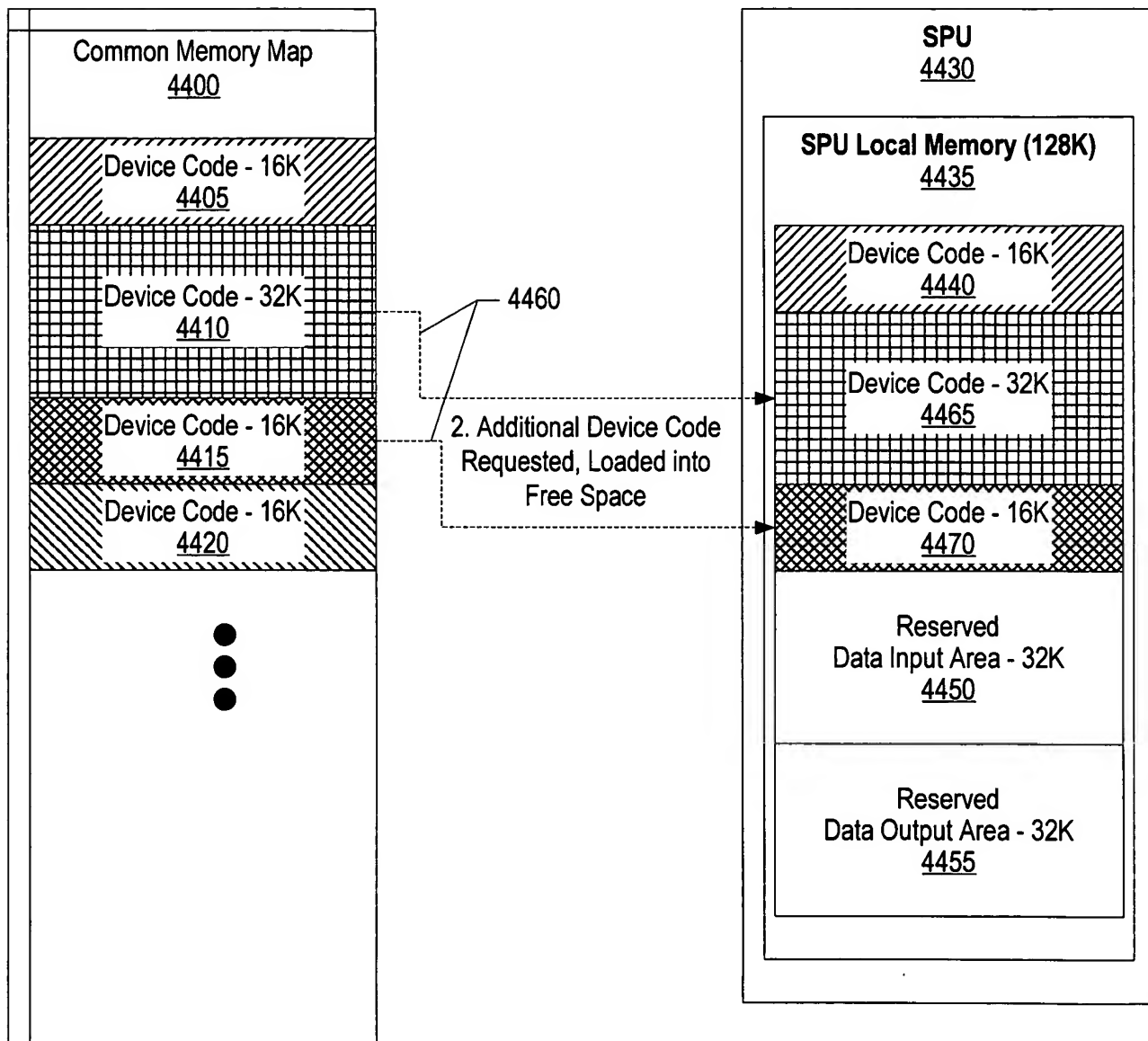


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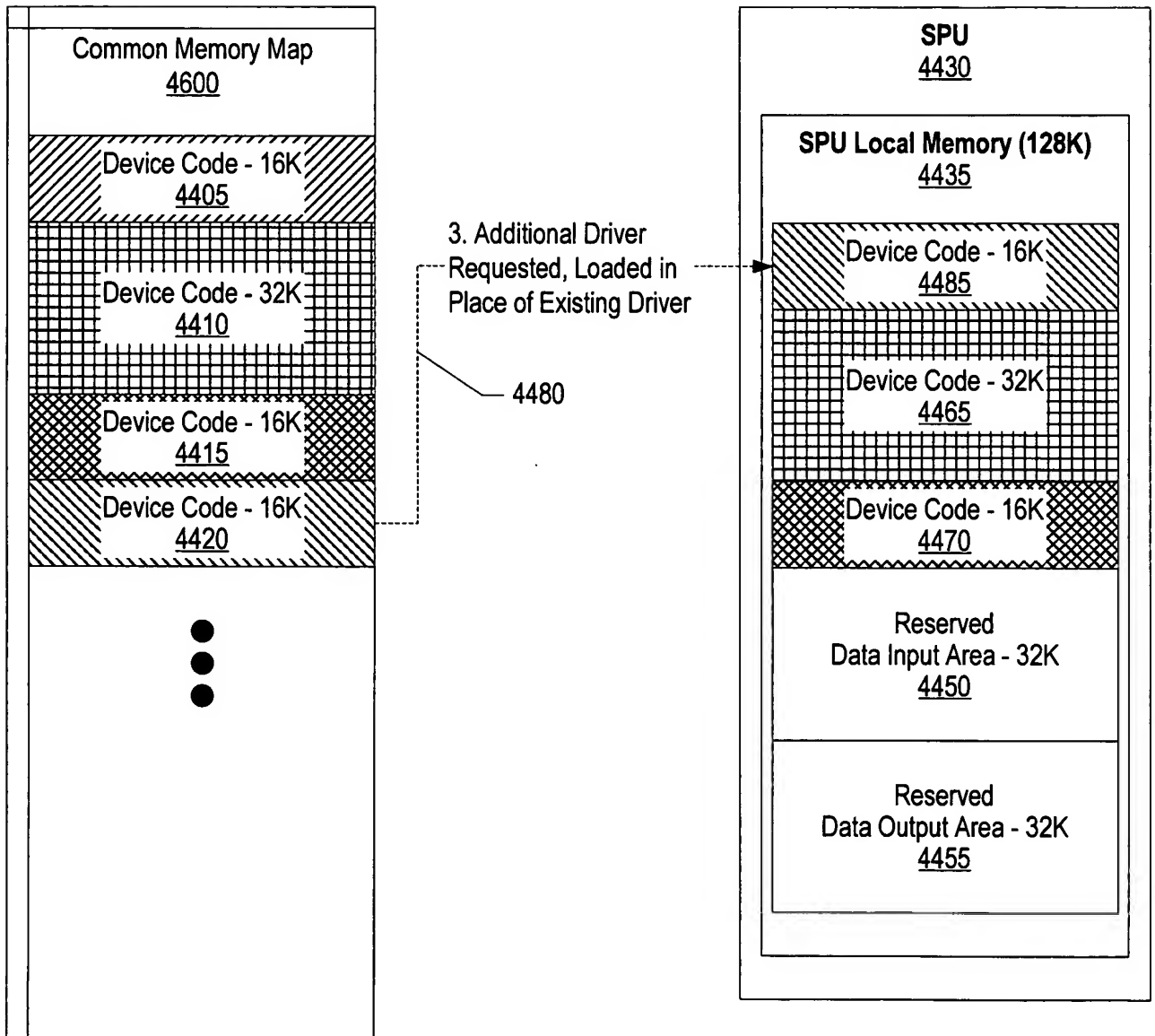
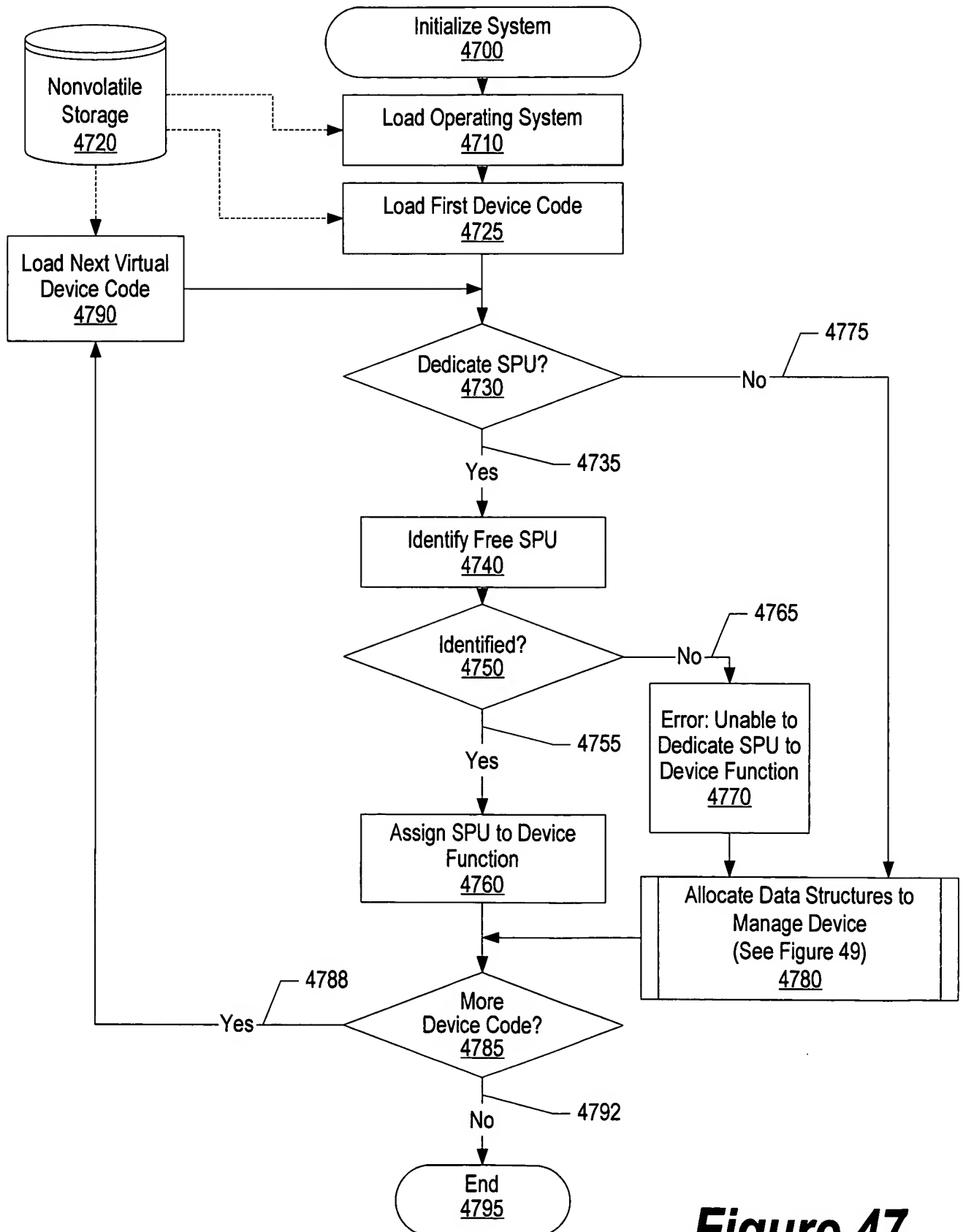


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**Figure 47**

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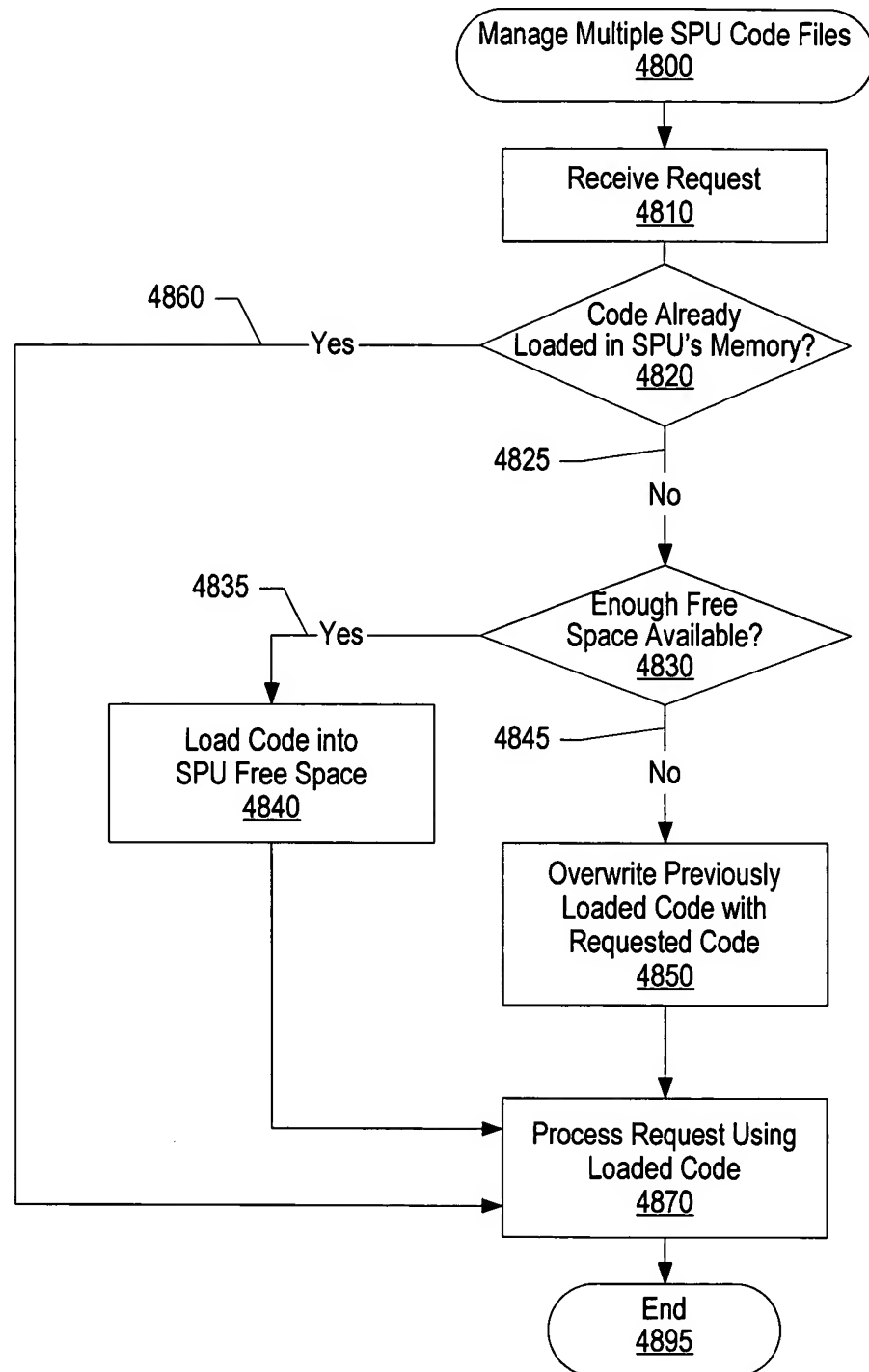


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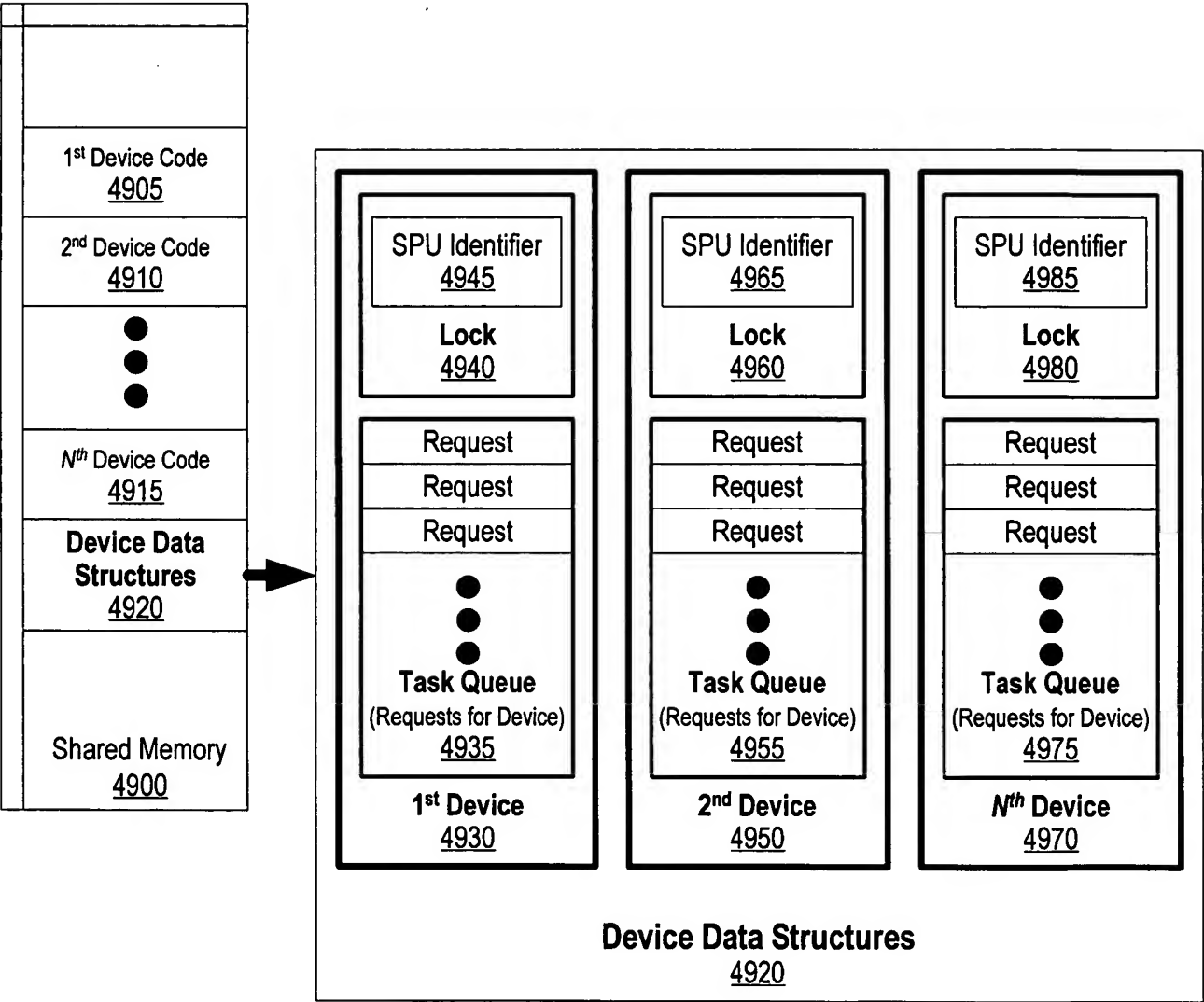
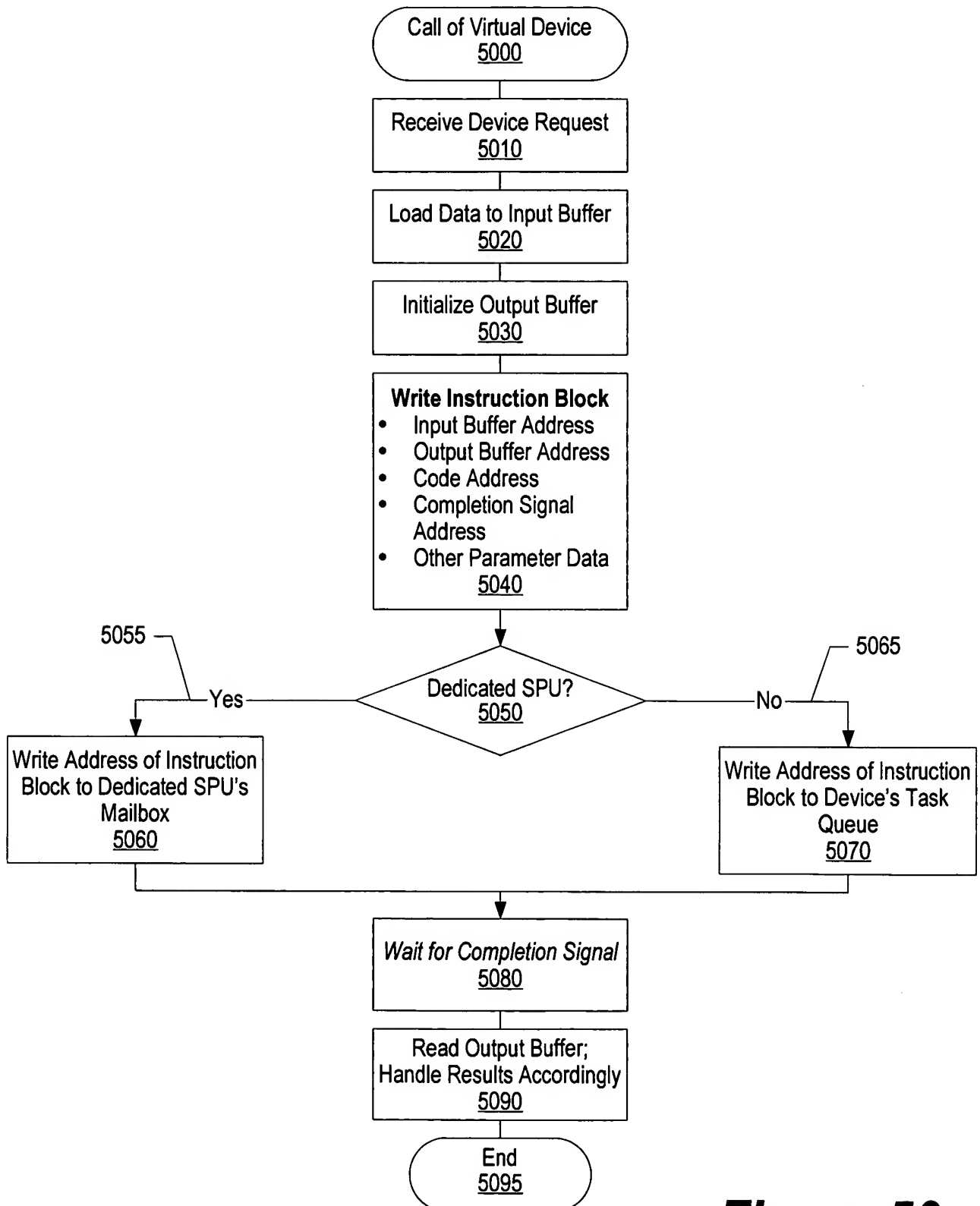
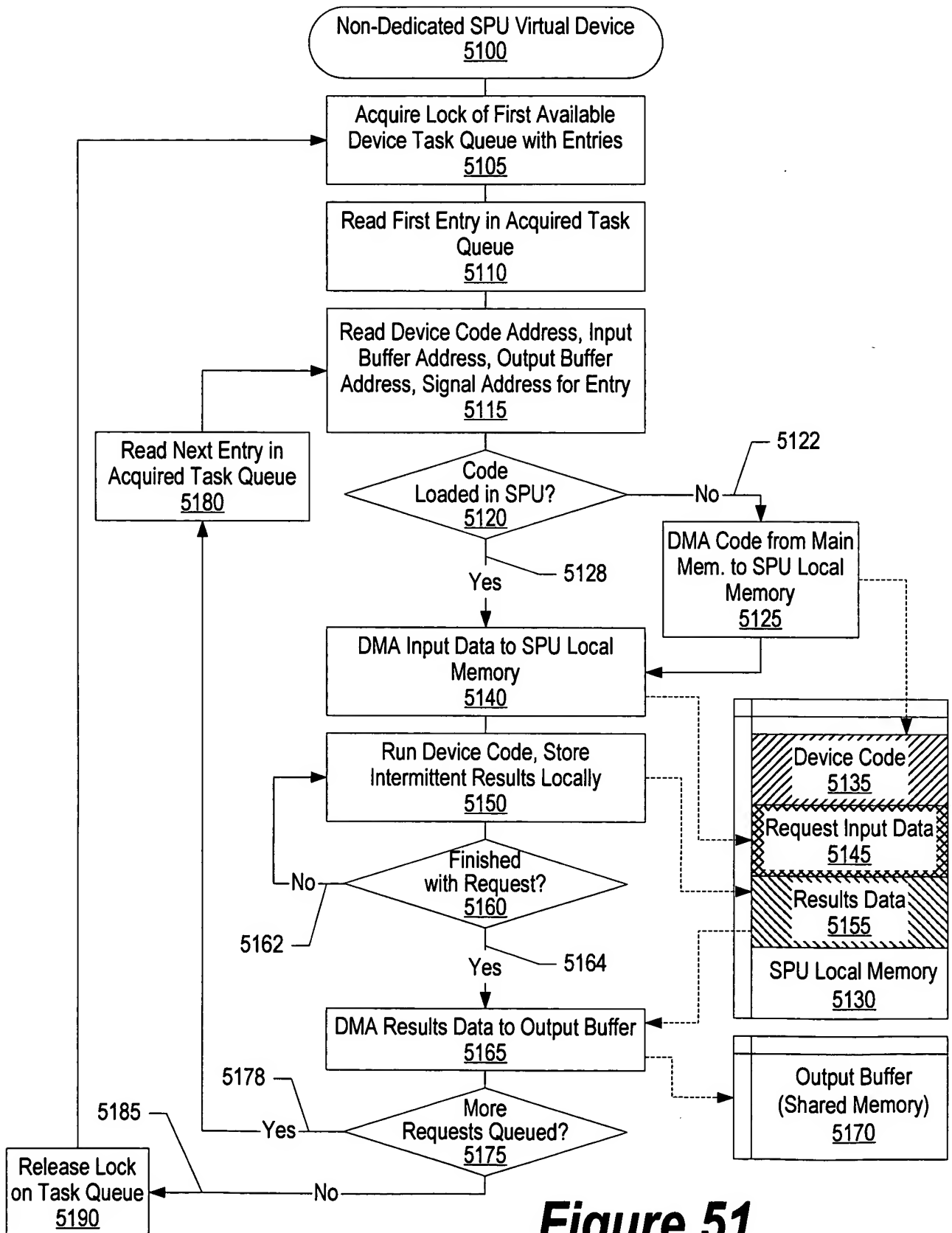


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**Figure 50**

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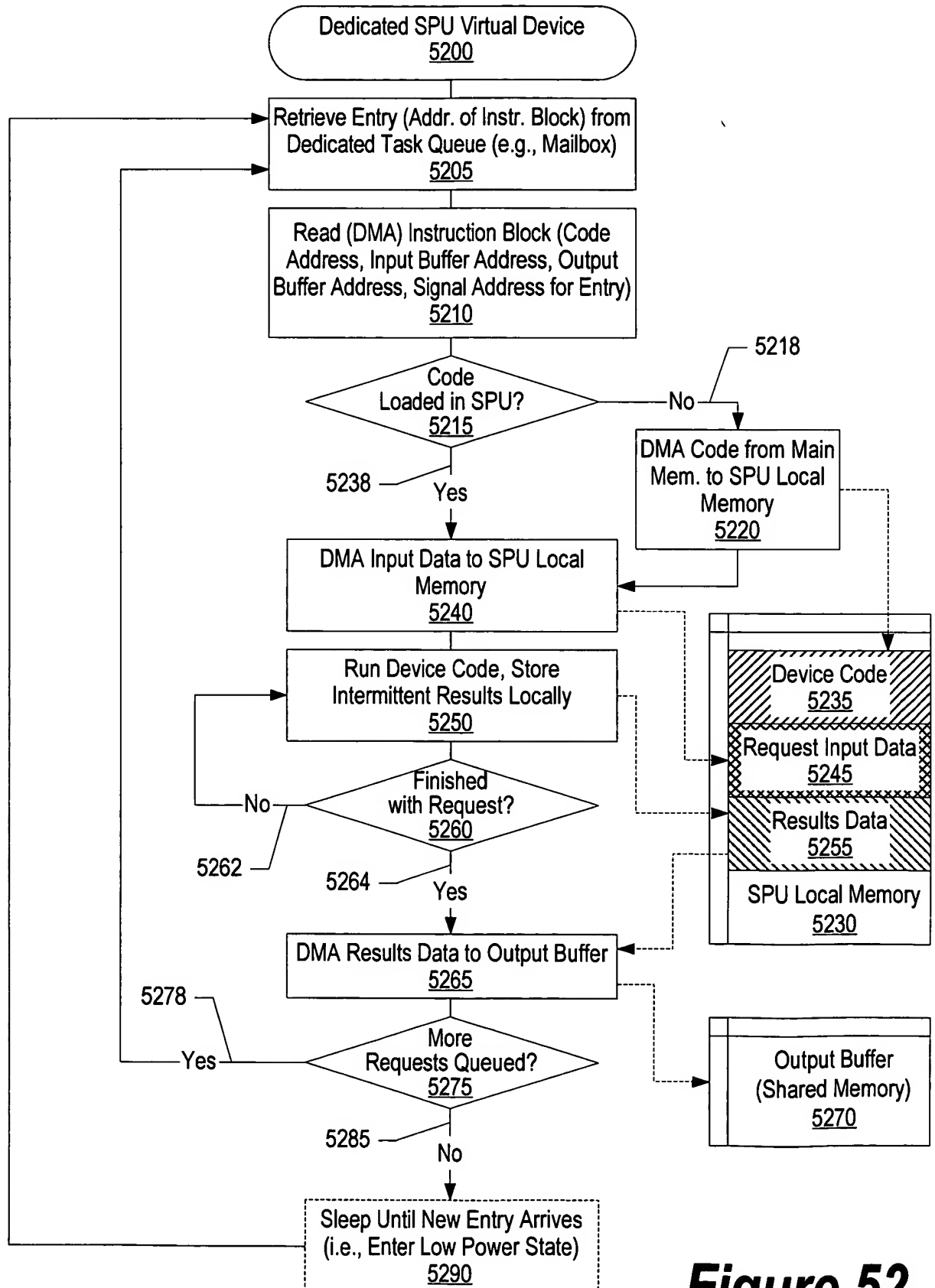
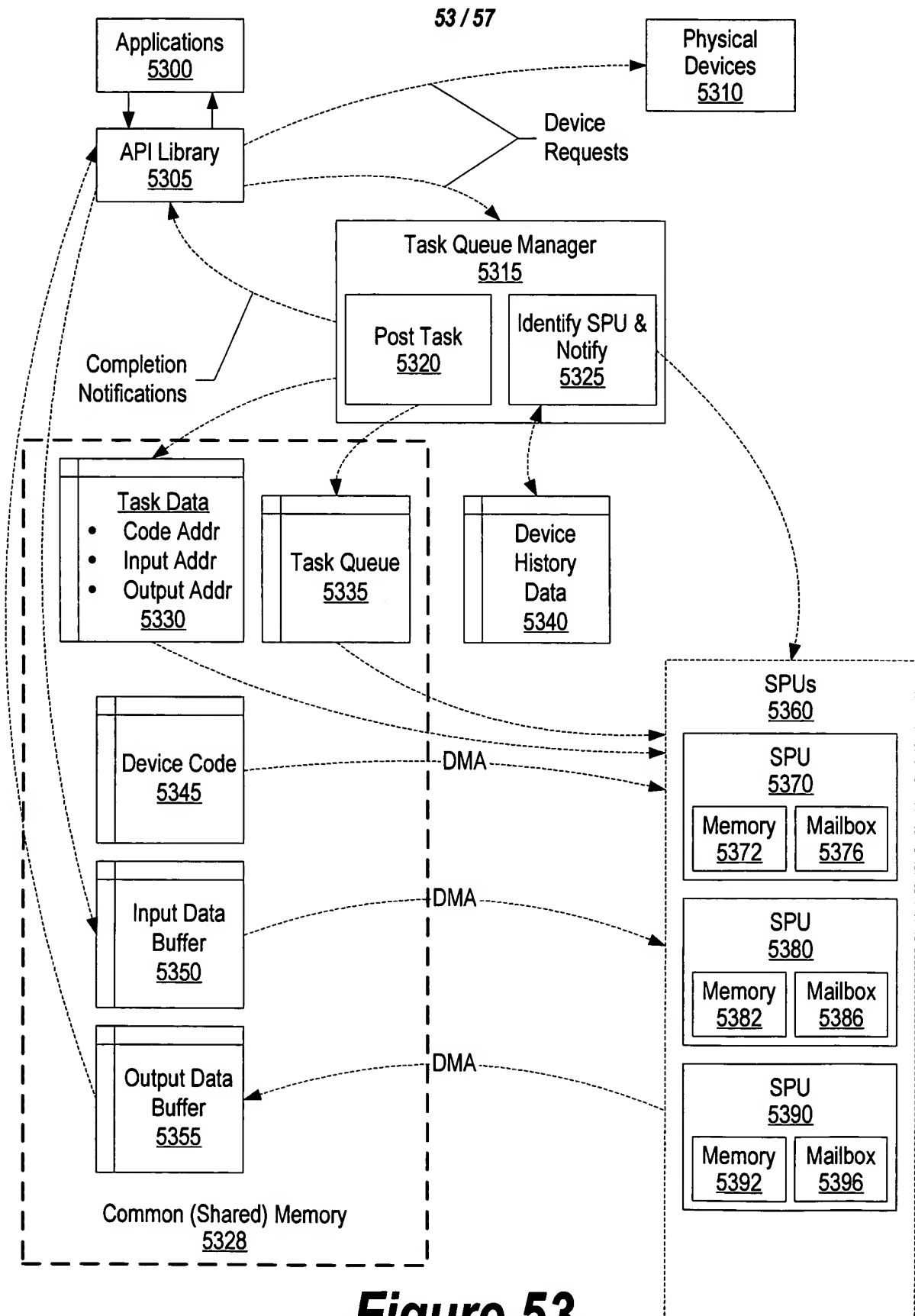
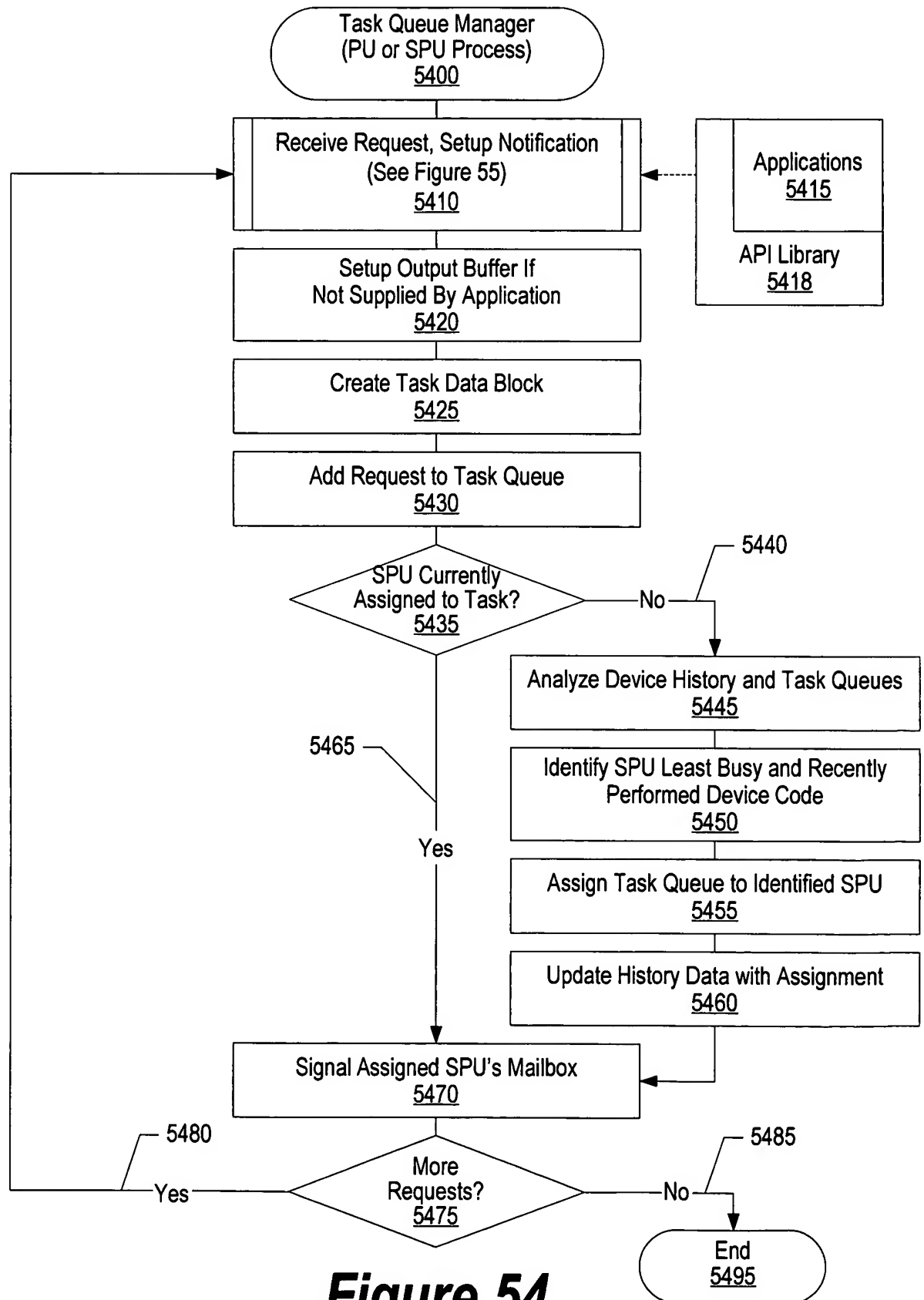


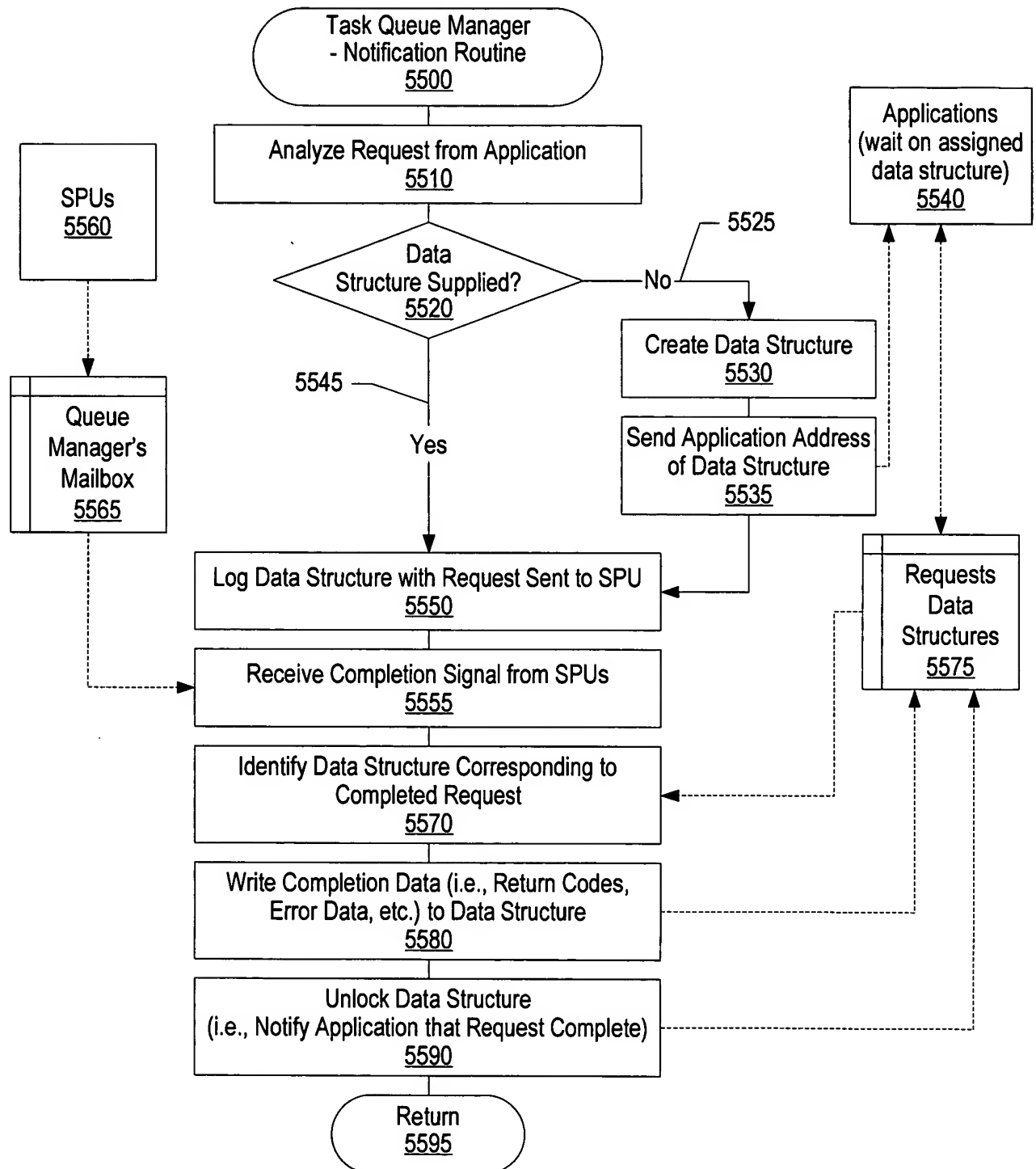
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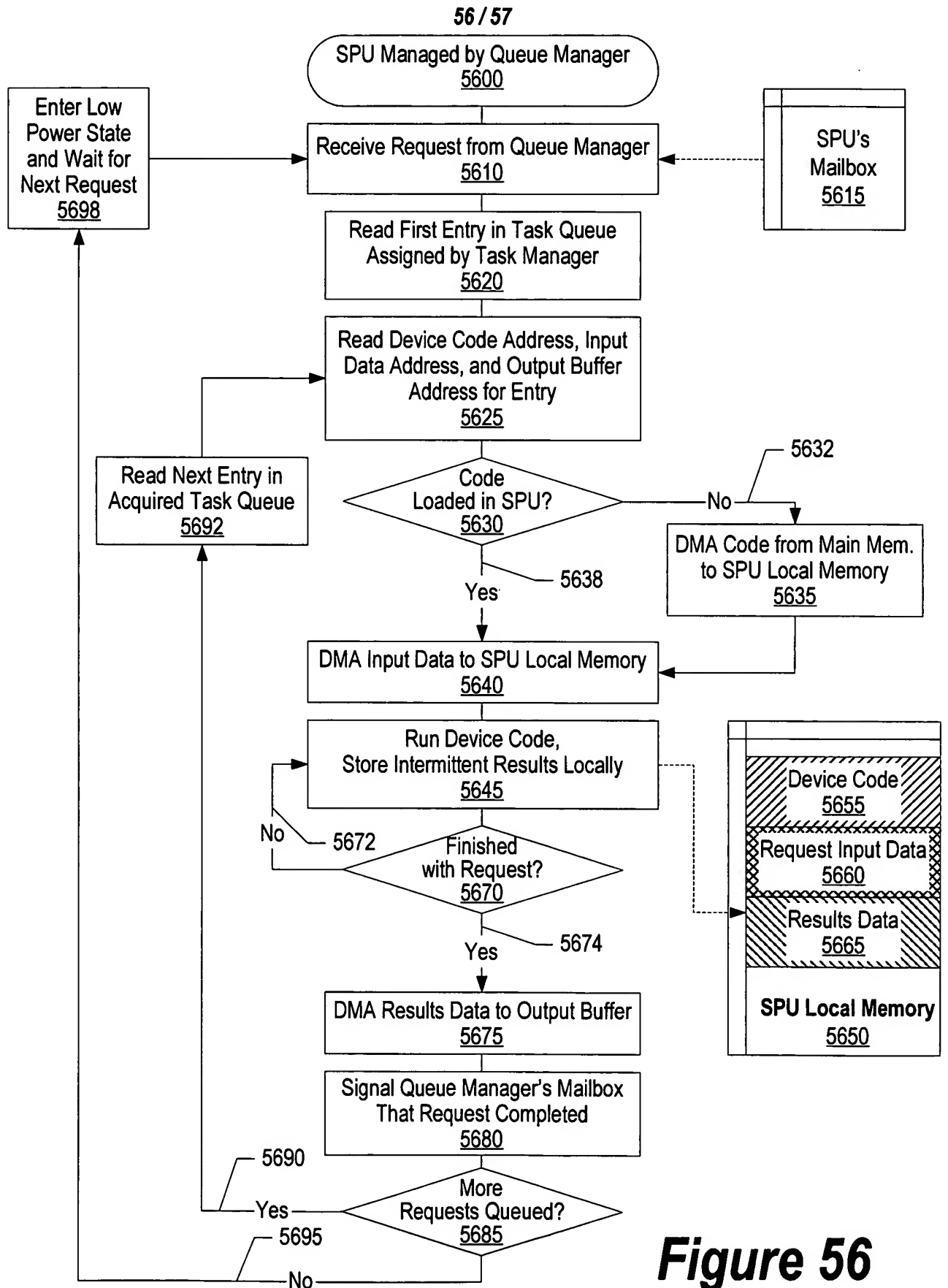


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**Figure 54**

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**Figure 55**



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